

## CPE690 Project #3

Oct. 12, 2009

At this time your model should have 4 major sections.

- Radar front end or stimulus
- IQ Processor
- Matched filters, 1 per channel
- Array processor
- Range-doppler map output

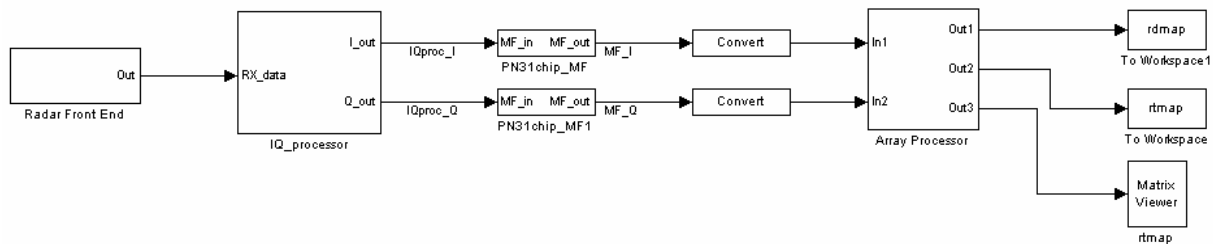


Figure 1: Notional radar receiver Simulink model

All simulation to this point was done in double precision, floating-point numbers.

For Project #3, convert the IQ Processor and Matched Filter to fixed point simulations. Provide a conversion back to double precision prior to array processing as shown in Figure 1.

Hints:

- Assume a 12-bit input from the radar front end. You must determine the binary scaling.
- Add a gain of 1000 Volts/Volts to the output of the test stimulus. This will move the stimulus into an appropriate range.
- Convert a small section, then run the model to verify it still works.

### Fixed-Point References

[1] S. K. Mitra. *Digital Signal Processing A Computer-Based Approach*. McGraw-Hill 2006

[2] R. Yates. "Fixed-Point Arithmetic: An Introduction". <http://www.digitalsignallabs.com>

[3] R. Yates "Practical Considerations in Fixed-Point FIR Implementations". <http://www.digitalsignallabs.com>

[4] Woods et al. *FPGA-based implementation of Signal Processing Systems*. Wiley 2008

[5] "AN083 Binary Numbering Systems", Altera Corporation