CPE 628
Chapter 5 – Logic Built-In Self-Test

Dr. Rhonda Kay Gaede

UAH

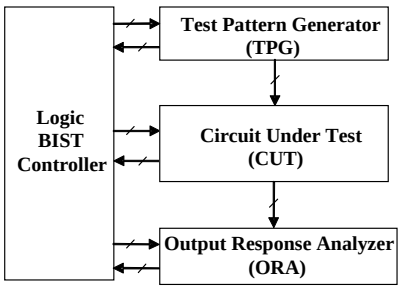
5.1 Introduction

- Introduce the basic concepts of _____ BIST
- BIST _____ Rules
- Test pattern generation and output _____ _____ techniques
- Fault Coverage _____
- Various BIST _____ _____ diagrams
- A Design Practice

4.1 Introduction – Logic BIST Techniques

- Why do we need built-in self-test (BIST)?
  - For _____ applications
  - Detect _____ faults
  - Provide _____ diagnosis
- _____ BIST
  - Concurrent online BIST
  - Non Concurrent online BIST
- _____ BIST
  - Functional offline BIST
  - Structural offline BIST

4.1 Introduction – Typical ATPG System



Structural off-line BIST

5.2 BIST Design Rules

Logic BIST requires much more _____ design restrictions when compared to conventional scan. Therefore, when designing a logic BIST system, it is essential that the circuit under test meet all _____ _____ *rules* and _____ _____ *design rules*, called _____ design rules.

One of the biggest problems is _____ values. Depending on the nature of each _____ _____, several _____ methods can be appropriate for use.

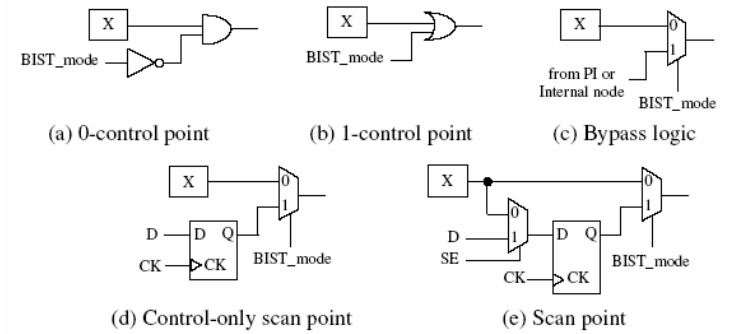
Common problems:

(1) _____.
(2) _____.

5.2 BIST Design Rules – Typical Unknown Sources

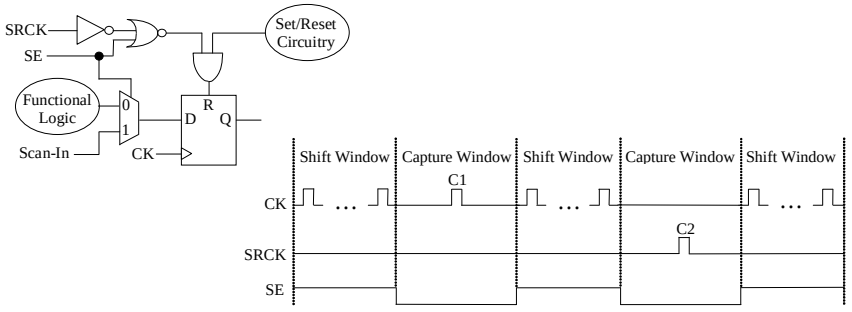
- _____
  - Adding bypass logic.
  - Adding control-only scan point
- _____
  - Bypass logic
  - Initialization
- _____
  - Scan points

5.2 BIST Design Rules – Unknown Source Blocking



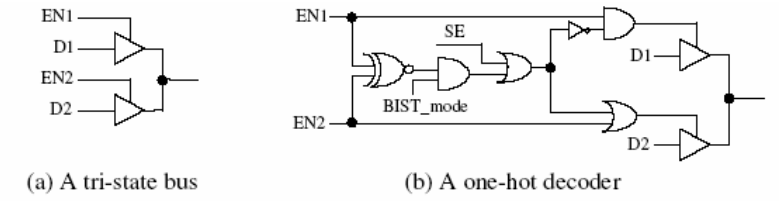
5.2 BIST Design Rules – Asynchronous Set/Reset Signals

- **Asynchronous Set/Reset Signals**
  - using the existing scan enable (SE) signal to protect each shift operation and adding a **set/reset clock point** (SRCK) on each set/reset signal to test the set/reset circuitry.



5.2 BIST Design Rules – Tri-State Buses

- **Tri-State Buses**
  - Re-synthesize each bus with _____.
  - _____ decoder

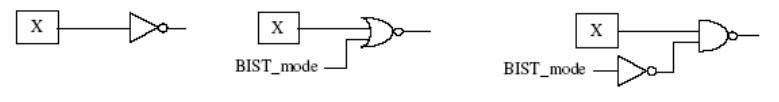


(a) A tri-state bus (b) A one-hot decoder

A _____ _____ for testing a tri-state bus with 2 drivers

5.2 BIST Design Rules

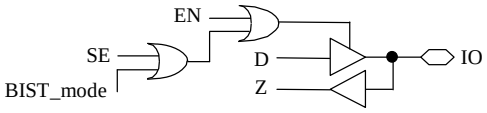
- **_____ Paths**
  - 0-control point
  - 1-control point
- **_____ Paths**
  - Adding an extra _____ ____ to a selected combinational gate on the _____ path



(a) An inverter (b) Embedded 0-control point (c) Embedded 1-control point

5.2 BIST Design Rules

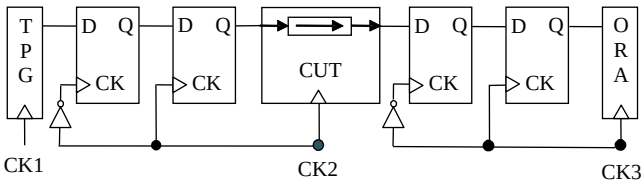
- _____ **I/O Ports**
  - Fix the _____ of each bi-directional I/O port to either input or output mode.



Forcing a bi-directional port to _____ mode

5.2 BIST Design Rules

_____ and _____ caused by clock _____ may occur between the TPG and the (scan chain) inputs of the CUT as well as between the (scan chain) outputs of the CUT and the ORA. To avoid these potential problems and ease physical implementation, we recommend adding _____ logic between the TPG and the CUT and between the CUT and the ORA.



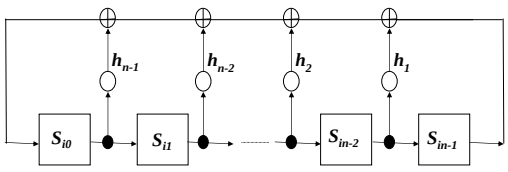
_____ ***logic among the TPG, CUT, and ORA***

5.3 Test Pattern Generation

- Test pattern generators (TPGs) constructed from _____ _____ shift registers (LFSRs)
- TPG
  - _____ testing (_____ set of tests)
  - Pseudo-_____ testing (_____ of tests plus _____ simulation)
  - Pseudo-_____ testing (_____ set of tests for ____ of each output)

5.3 Test Pattern Generation – Standard LFSR(External XOR)

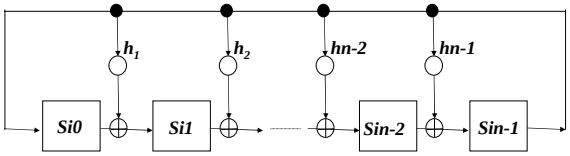
Consists of *n* __ _____ and a _____ number of exclusive-OR (XOR) gates



5.3 Test Pattern Generation – Standard LFSR(Internal XOR)

•Each XOR gate placed between two _____ D flip-flops

•At most, one _____ of ____ delay



5.3 Test Pattern Generation – Standard LFSR(Characteristic Polynomial)

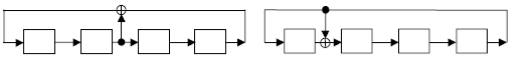
- The internal _____ of the *n*-stage LFSR can be described by a _____ polynomial of degree *n*,

  $f(x) = 1 + h_1x + h_2x^2 + \ldots + h_{n-1}x^{n-1} + x^n$,

  where h represents a _____ in the circuit.
- Let S_i represent the _____ of the *n*-stage LFSR after *i* _____ of the _____ contents,S_0,of the LFSR, and $S_i(x)$ be the polynomial representation of S_i

  $S_i(x) = S_{i0} + S_{i1}x + S_{i2}x^2 + \ldots + S_{in-2}x^{n-2} + S_{in-1}x^{n-1}$
- If T is the _____ _____ integer such that f(x) divides $1 + x^T$,then the integer T is called the _____ of the LFSR.
- If $T = 2^n - 1$, then the n-stage LFSR generates a _____-length sequence.

5.3 Test Pattern Generation – Standard LFSR(Maximal Length LFSR)



(a) A 4-stage standard LFSR (b) A 4-stage modular LFSR

(c) Test sequence generated by (a)	(d) Test sequence generated by (b)
0 0 0 1	**0 0 0 1**
1 0 0 0	1 1 0 0
0 1 0 0	0 1 1 0
1 0 1 0	0 0 1 1
0 1 0 1	1 1 0 1
0 0 1 0	1 0 1 0
0 0 0 1	0 1 0 1
1 0 0 0	1 1 1 0
0 1 0 0	0 1 1 1
1 0 1 0	1 1 1 1
0 1 0 1	1 0 1 1
0 0 1 0	1 0 0 1
0 0 0 1	1 0 0 0
1 0 0 0	0 1 0 0
0 1 0 0	0 0 1 0
1 0 1 0	**0 0 0 1**

a. $f(x) = 1 + x^2 + x^4$

b. $f(x) = 1 + x + x^4$

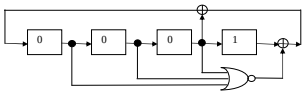
$S_0 = x^3$

5.3 Test Pattern Generation – Standard LFSR(Primitive Polynomials)

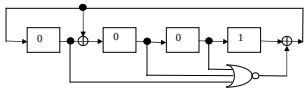
n	Exponents	n	Exponents	n	Exponents	n	Exponents
1	0	26	8 7 1 0	51	16 15 1 0	76	36 35 1 0
2	1 0	27	8 7 1 0	52	3 0	77	31 30 1 0
3	1 0	28	3 0	53	16 15 1 0	78	20 19 1 0
4	1 0	29	2 0	54	37 36 1 0	79	9 0
5	2 0	30	16 15 1 0	55	24 0	80	38 37 1 0
6	1 0	31	3 0	56	22 21 1 0	81	4 0
7	1 0	32	28 27 1 0	57	7 0	82	38 35 3 0
8	6 5 1 0	33	13 0	58	19 0	83	46 45 1 0
9	4 0	34	15 14 1 0	59	22 21 1 0	84	13 0
10	3 0	35	2 0	60	1 0	85	28 27 1 0
11	2 0	36	11 0	61	16 15 1 0	86	13 12 1 0
12	7 4 3 0	37	12 10 2 0	62	57 56 1 0	87	13 0
13	4 3 1 0	38	6 5 1 0	63	1 0	88	72 71 1 0
14	12 11 1 0	39	4 0	64	4 3 1 0	89	38 0
15	1 0	40	21 19 2 0	65	18 0	90	19 18 1 0
16	5 3 2 0	41	3 0	66	10 9 1 0	91	84 83 1 0
17	3 0	42	23 22 1 0	67	10 9 1 0	92	13 12 1 0
18	7 0	43	6 5 1 0	68	9 0	93	2 0
19	6 5 1 0	44	27 26 1 0	69	29 27 2 0	94	21 0
20	3 0	45	4 3 1 0	70	16 15 1 0	95	11 0
21	2 0	46	21 20 1 0	71	6 0	96	49 47 2 0
22	1 0	47	5 0	72	53 47 6 0	97	6 0
23	5 0	48	28 27 1 0	73	25 0	98	11 0
24	4 3 1 0	49	9 0	74	16 15 1 0	99	47 45 2 0
25	3 0	50	27 26 1 0	75	11 10 1 0	100	37 0

- A maximal length LFSR is constructed using _____ polynomials.
- A _____ polynomial is a polynomial that divides _____ but not _____, for any integer $i < T$, where $T = 2^n-1$.
- Maximal length LFSRs leave out one pattern, ___ _____.

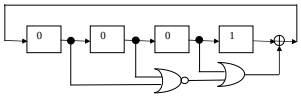
5.3 Test Pattern Generation – Standard LFSRs(Complete LFSRs)



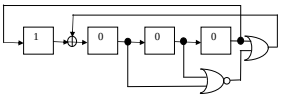
(a) 4-stage standard CFSR



(b) 4-stage modular CFSR



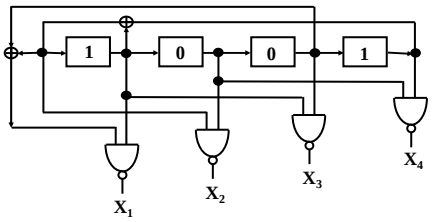
(c) A minimized version of (a)



(d) A minimized version of (b)

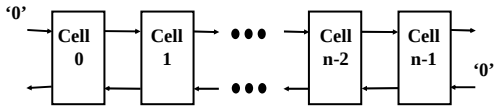
5.3 Test Pattern Generation – Pseudo-Random Testing

- **Exhaustive Testing works well for _____.**
- **Pseudo-Random generates a subset using a maximum-length LFSR.**
- **Each maximum-length LFSR produces a sequence with ____ probability of generating _____ at every output.**
- **For _____ _____ faults, you can use logic to _____ the patterns.**

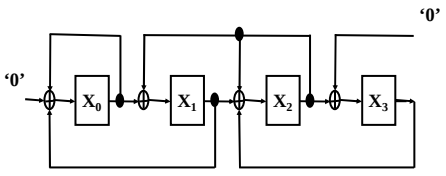


5.3 Test Pattern Generation – Pseudo-Random Testing (Cellular Automata)

- Provide _____ _____ test patterns
- Provide _____ _____ coverage in a random-pattern resistant (RP-resistant) circuit
- Implementation advantage
- General structure of an n-stage cellular automata
  - Rule 90: $x_i(t+1) = x_{i-1}(t) + x_{i+1}(t)$
  - Rule 150: $x_i(t+1) = x_{i-1}(t) + x_i(t) + x_{i+1}(t)$



5.3 Test Pattern Generation – Pseudo-Random Testing (Cellular Automata Example)



0 0 0 1
0 0 1 0
0 1 1 1
1 1 1 1
0 0 1 1
0 1 0 1
1 0 0 0
1 1 0 0
0 1 1 0
1 1 0 1
0 1 0 0
1 0 1 0
1 0 1 1
1 0 0 1
1 1 1 0

5.3 Test Pattern Generation – Pseudo-Exhaustive Testing

- Reduce _____ _____ while retaining many advantages of _____ testing
- Guarantee 100% single-stuck fault coverage
  - _____ test technique
  - _____ test technique

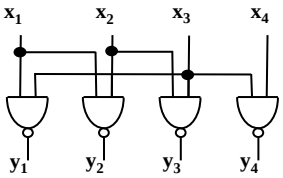
5.3 Test Pattern Generation – Pseudo-Exhaustive Testing (Verification Testing)

- _____ the CUT into m cones, _____ from each output to determine the inputs that drive the output.
- Each cone will receive _____ test patterns and are tested _____.
- Pseudo-exhaustive pattern generation techniques
  - _____
  - _____
  - _____
  - _____
  - _____
  - _____
  - _____

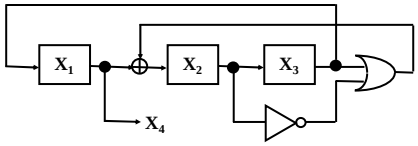
5.3 Test Pattern Generation – Syndrome Driver Counter

Use SDC to generate test patterns. Check whether some inputs can _____ the same test signal. If *n-p* Inputs can share test inputs with other *p* inputs, then the circuit can be tested exhaustively with these *p* inputs. In this case, __ and __ can share a test signal.

An (n, w)=(4, 2) CUT



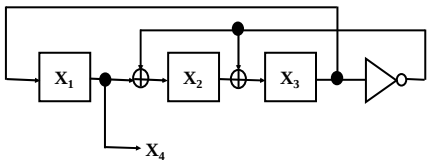
0010
1001
1101
1111
0110
1011
0100



5.3 Test Pattern Generation – Constant-Weight Counter

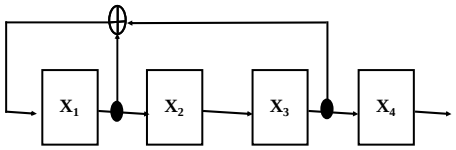
Use CWCs to generate test patterns. Constant-Weight counters are constructed using *constant-weight code* or _____ *code.* The constant-weight test set is a _____-length test set for many circuits.

1101
0000
0110
1011



5.3 Test Pattern Generation – Combined LFSR/SR

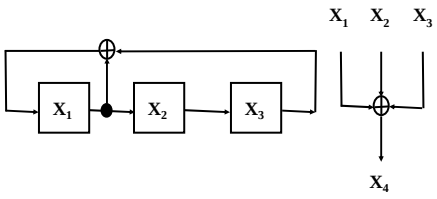
Use a combination of an LFSR and a shift register (SR) for pattern generation. The method is most effective when __ is much less than __. In general, this technique requires ____ ____ tests than other schemes when __ is greater than ___. However, it usually requires at least ____ seeds. This sequence can test the (4,2) circuit because the _____ patterns occur on all _____ of outputs.



1100
1110
0111
1011
0101
0010
1001

5.3 Test Pattern Generation – Combined LFSR/Phase Shifter

A combined LFSR/PS approach using a combination of an LFSR and a linear phase shifter which includes a _____ of ____ gates to generate test pattern. Similar to combined LFSR/SR, this technique requires more tests than other schemes when *w* is greater than *n/2*. Again, any two outputs contain all four combinations. The number of seeds required is __ ____ two.



1100
1111
0110
1010
0101
0011
1001

5.3 Test Pattern Generation – Condensed LFSR

Condensed LFSRs are constructed based on _____ codes.

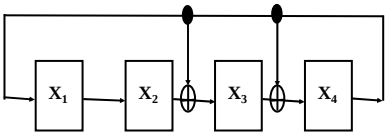
Define *g(x)* and *p(x)* as the _____ polynomial and _____ polynomial over GF(2), respectively. An *(n, k)* condensed LFSR can be realized using

$$f(x) = g(x)p(x) = (1 + x + x^2 + \ldots + x^{n-k})p(x)$$

where

$$w < \lceil k/(n - k \_ 1) \rceil + \lfloor k/(n - k + 1) \rfloor$$

(4,3) with $S_0(x) = g(x) = 1 + x$ for testing (n,w) = (4, 2) CUT



1100
0110
0011
1010
0101
1001
1111

5.3 Test Pattern Generation – Cyclic LFSR

Use cyclic LFSRs to reduce the test length when _____.

A cyclic code always exists when n' = _____, _____

To exhaustively test any *(n,w)* CUT

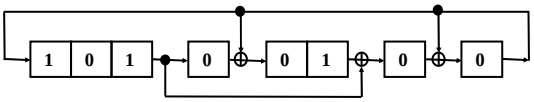
- -find a generator polynomial *g(x)* of _____ degree __ (or _____ degree __), for generating an *(n',k') = (n',n'-k)* cyclic code, that divides _____ and has a design distance _____;
- –construct an (n',k) cyclic LFSR using
  $$f(x) = h(x)p(x) = (1+x^{n'})p(x)/g(x), \text{ where } h(x) = (1+x^{n'})/g(x);$$
- -shorten this *(n',k)* cyclic LFSR to an *(n,k)* cyclic LFSR by deleting the _____, _____, or _____ *n'-n* stages from the *(n',k)* cyclic LFSR.

To test a _____ CUT, no cyclic code for 8, use n' = ___ and k' = ___

5.3 Test Pattern Generation – Cyclic LFSR (Example)

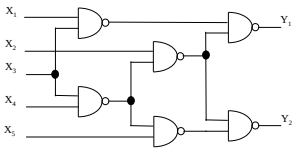
To test a _____ CUT, no cyclic code for 8, use n' = ___ and k' = ___

A (8,5) cyclic LFSR, picking the first ___stages and the last ___ stages of the (15,5) cyclic LFSR, has a period of ___

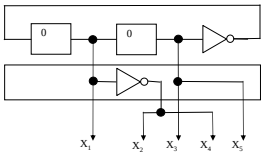


5.3 Test Pattern Generation – Compatible LFSR

The combined LFSR of an *l*-stage LFSR and an *l-to-n* _____ logic, called *l*-stage compatible LFSR, can further _____ the test length, when only _____ stuck faults are considered.



(a) An (n,w) = (5,4) CUT



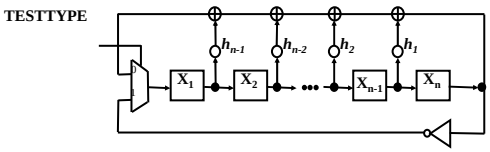
(b) A 2-stage compatible LFSR

5.3 Test Pattern Generation – Segmentation Testing

- Used when
  - Test _____ using previous techniques is too _____ or
  - Output depends on ____ inputs.
- Divide the circuit into segments
  - _____ partitioning
  - _____ partitioning

5.3 Test Pattern Generation – Delay Fault Testing

- Need _____ patterns to test delay fault exhaustively
- Test set could cause test _____ when more than _____ input changes.
- Use maximal LFSR plus _____ counter to generate $2n(2^n - 1)$ _____ patterns



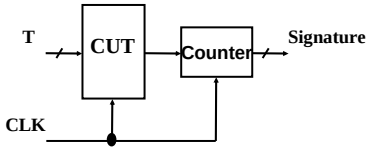
5.4 Output Response Analysis

- Output responses are _____ into a signature
- _____ is different from _____, _____ is lossy.
- Compaction techniques
  - ____ _____ testing
  - _____ _____ testing
  - _____ _____

5.4 Output Response Analysis – Ones Count Testing

Assume the CUT has ___ output and the output contains a stream of *L* bits. Let the fault-free output response be $\{r_0, r_1, r_2, \ldots, r_{L-1}\}$ Ones count testing will need a counter to count ___ _____ ___ ___ in the bit stream.

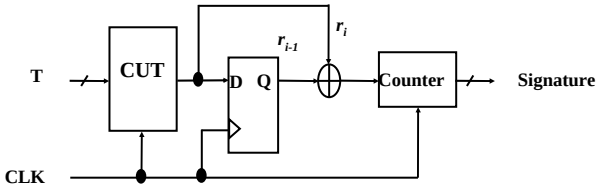
The _____ probability $P_{OC}(m) = (C(L,m)-1)/(2^L - 1)$ where m is the _____ number of _____ and C(L, m) is the combination of ___ taken ___ at a time and L is the _____ of the sequence.



5.4 Output Response Analysis - Transition Count Testing

Transition count testing is similar to that for ones count testing, except the _____ is defined as the number of *1-to-0* and *0-to-1* _____.

The aliasing probabilty is $P_{TC}(m) = (2C(L-1,m)-1)/(2^L-1)$ where m is the fault-free number of _____ and C(L-1, m) is the combination of L-1 taken m at a time and L is the length of the sequence.

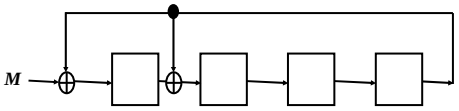


5.4 Output Response Analysis – Signature Analysis

Signature analysis is the _____ _____ compaction technique used today, based on _____ _____ checking.

Two signature analysis schemes
_____ signature analysis (_____)
_____ signature analysis (_____)

5.4 Output Response Analysis – Signature Analysis (Serial Example)



M	r_0	r_1	r_2	r_3
1	**0**	**0**	**0**	**0**
1	1	0	0	0
0	1	1	0	0
1	0	1	1	0
1	1	0	1	1
0	0	0	0	1
0	1	1	0	0
1	0	1	1	0
R	**1**	**0**	**1**	**1**

(a) Fault-free signature

M'	r_0	r_1	r_2	r_3
1	**0**	**0**	**0**	**0**
1	1	0	0	0
0	1	1	0	0
1	0	1	1	0
0	1	0	1	1
0	1	0	0	1
1	1	0	0	0
1	1	1	0	0
R'	**1**	**1**	**1**	**0**

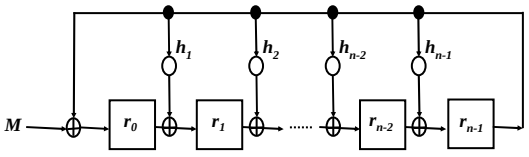
(b) Signature for fault f_1

M''	r_0	r_1	r_2	r_3
1	**0**	**0**	**0**	**0**
0	1	0	0	0
1	0	1	0	0
1	1	0	1	0
0	1	1	0	1
0	1	0	1	0
1	0	1	0	1
1	0	1	1	0
R''	**1**	**0**	**1**	**1**

(c) Signature for fault f_2

5.4 Output Response Analysis – Signature Analysis (Serial)

An n-stage single-input signature register



Define *L-bit* output sequence *M*

$$M(x) = m_0 + m_1 x + m_2 x + \ldots + m_{L-1} x^{L-1}$$

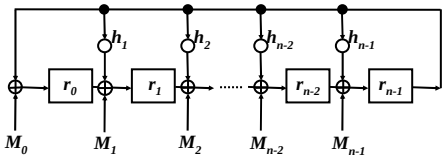
Let the polynomial of the modular LFSR be *f(x)*

Aliasing Probability

IF M(x) = q(x) f(x) + r(x) ⇒ Signature is the polynomial remainder, *r(x)*

5.4 Output Response Analysis – Signature Analysis (Parallel)

Multiple-input signature register (_____)

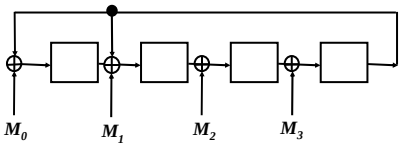


An n-input MISR can be remodeled as a single-input SISR with _____ _____ *sequence M(x)* and _____ _____ _____ *E(x)*

$$M(x) = M_0(x) + xM_1(x) + \ldots + x^{n-2}M_{n-2}(x) + x^{n-1}M_{n-1}(x)$$

$$E(x) = E_0(x) + xE_1(x) + \ldots + x^{n-2}E_{n-2}(x) + x^{n-1}E_{n-1}(x)$$

5.4 Output Response Analysis – Signature Analysis (Parallel Example)



A 4-stage MISR

M_0	1 0 0 1 0
M_1	0 1 0 1 0
M_2	1 1 0 0 0
M_3	1 0 0 1 1
M	1 0 0 1 1 0 1 1

An equivalent M sequence

Aliasing probability

$$P_{PSA}(n) = (2^{(mL-n)} - 1)/(2^{mL} - 1)$$

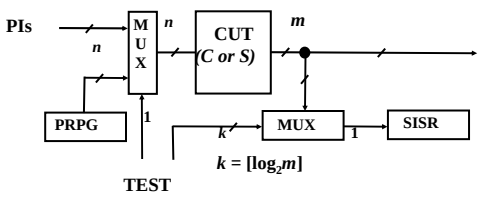
5.5 Logic BIST Architectures

Four Types of BIST Architectures:

- No _____ structure to the CUT
- Make use of ____ _____ in the CUT
- _____ the scan chains for test pattern _____ and output response _____
- Use concurrent _____ circuitry of the design

5.5 Logic BIST Architectures – BIST Architectures for Non-scan Circuits

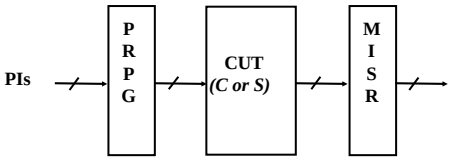
Two LFSRs and two multiplexers are added to the circuit. The first LFSR acts as a _____, the second serves as a _____. The first multiplexer selects the inputs, another routes the PO to the SISR.



CSBL Architecture

5.5 Logic BIST Architectures – BIST Architectures for Non-scan Circuits

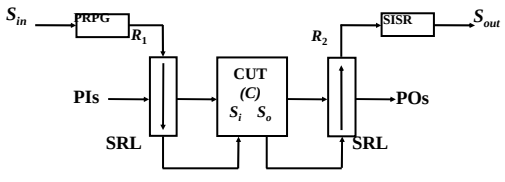
Use a PRPG and a MISR. Pseudo-random patterns are applied in parallel from the PRPG to the chip primary inputs (PIs) and a MISR is used to compact the chip output responses.



BEST Architecture

5.5 Logic BIST Architectures – BIST Architectures for Scan Circuits

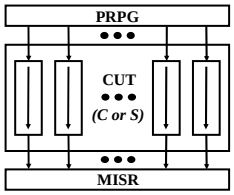
In addition to the internal scan chain, an external scan chain comprising all _____ _____ and _____ _____ is required. The external scan-chain input is connected to the the internal scan chain.



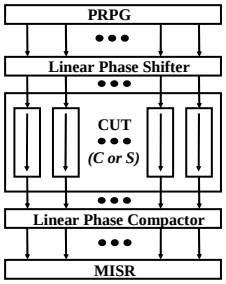
LOCST Architecture

5.5 Logic BIST Architectures – BIST Architectures for Scan Circuits

Contains a PRPG (SRSG) and a MISR. The ____ _____ are loaded in parallel from the PRPG. The _____ clocks are then pulsed and the ____ _____ are scanned out to the MISR for compaction. New test patterns are scanned in at the _____ ____ as the test responses are being scanned out.

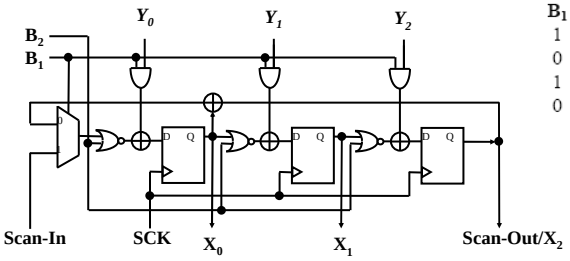


STUMPS



5.5 Logic BIST Architectures – BIST Architectures w/ Register Reconfiguration

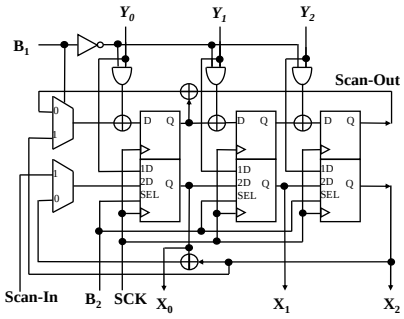
The architecture applies to circuits that can be partitioned into _____ _____ (logic blocks). Each module is assumed to have its own input and output _____ (_____ elements), or such _____ are added to the circuit where necessary. The registers are _____ so that for test purposes they act as PRPGs or MISRs.



B_1	B_2
1	1
0	0
1	0
0	1

BILBO

5.5 Logic BIST Architectures – BIST Architectures w/ Register Reconfiguration

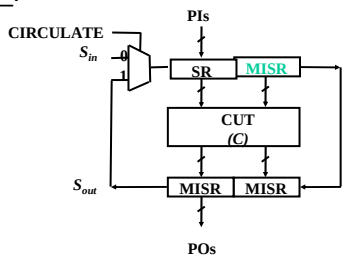


CBILBO

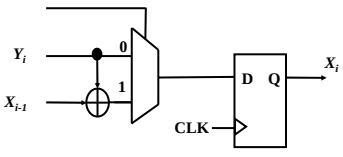
B_1	B_2	Operation mode
-	0	Normal
1	1	Scan
0	1	Test Generation and Signature Analysis

5.5 Logic BIST Architectures – BIST Architectures w/ Register Reconfiguration

All primary inputs and primary outputs are reconfigured as _____ scan cells. They are connected to the internal scan cells to form a _____ path. During _____, all primary inputs (PIs) are connected as a shift register (SR), whereas all internal scan cells and primary outputs (POs) are reconfigured as a MISR. Fault coverage is _____.

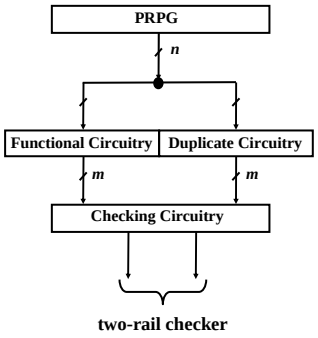


(a) The CSTP architecture



(b) Self-Test cell

5.5 Logic BIST Architectures – BIST Architectures w/ Concurrent Checking



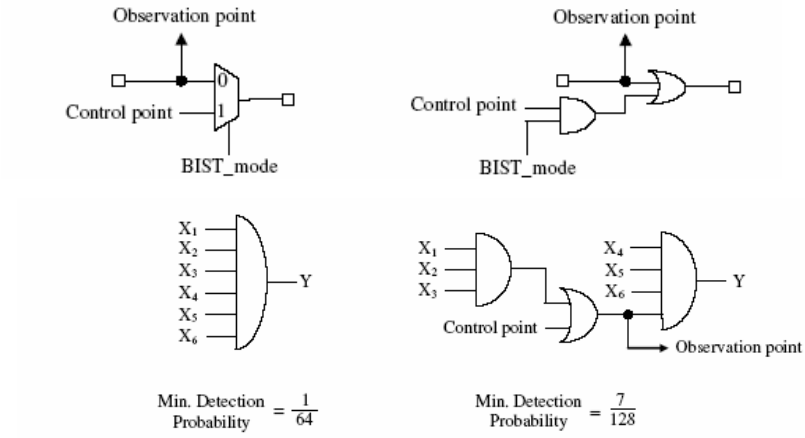
CSV Architecture

5.6 Fault Coverage Enhancement

Three approaches to enhance the fault coverage

- Test point insertion
- Mixed-mode BIST
- Hybrid BIST

5.6 Fault Coverage Enhancement – Test Point Insertion



(a) An output RP-resistant stuck-at-0 fault (b) Example inserted test points

5.6 Fault Coverage Enhancement – Test Point Insertion (Placement)

Where to place the test points in the circuit to maximize the coverage and minimize the number of test points required.

- _____ _____ guided techniques
- _____ _____ guided techniques
- _____ *test point insertion* technique

•During normal operation control points must be _____

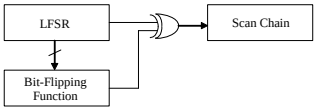
- Random
- Deterministic

5.6 Fault Coverage Enhancement – Mixed-Mode BIST (No Modification to CUT)

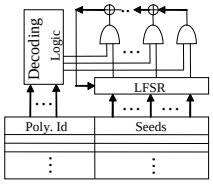
_____ patterns are generated to detect the RP-testable faults, and then some additional _____ patterns are generated to detect the RP-resistant faults.

Approaches

- ROM Compression – _____ _____
- LFSR Reseeding – also _____
- Embedding Deterministic Patterns



Bit-flipping BIST



Reseeding with multiple-polynomial LFSR

5.6 Fault Coverage Enhancement – Hybrid BIST (Load from Tester)

For _____ fault coverage enhancement where a tester is present, deterministic data from the tester can be used to improve the fault coverage.

- Top-up ATPG
- Store the _____ deterministic patterns on the tester

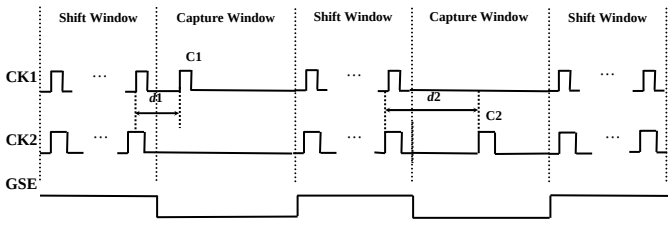
5.7 BIST Timing Control

- To test _____-clock-domain circuits
- To detect _____-clock-domain faults and _____-clock-domain faults
- Capture-clocking schemes
  - –Single-capture
  - –Skewed-load
  - –Double-capture

5.7 BIST Timing Control – One-Hot Single Capture

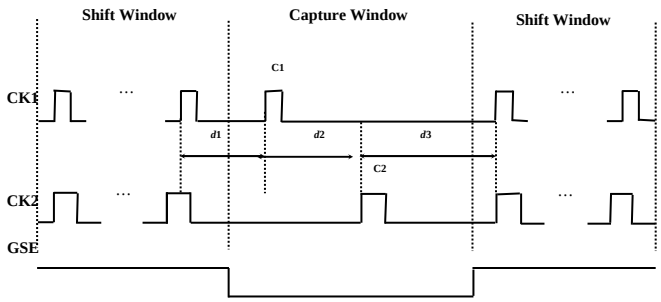
A capture pulse is applied to ___ _____ _____, while holding ____ _____ test clocks inactive, during each capture window.

Benefit: a single and slow _____ scan mode signal
Drawback: long test time



5.7 BIST Timing Control – Staggered Single Capture

Benefits: short test time; a _____ and ____ global scan mode signal
Drawback: some _____ fault coverage loss if the ordered sequence of capture clocks is _____ for all capture cycles



5.7 BIST Timing Control – Skewed-Load

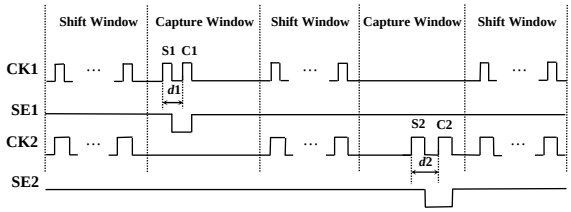
- An at-speed _____ test technique
- Address ____-clock-domain _____ faults
- Three approaches
  - One-hot skewed-load
  - Aligned skewed-load
  - Staggered skewed-load

5.7 BIST Timing Control – One-Hot Skewed-Load

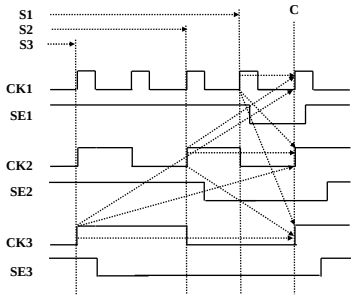
Tests all clock domains one by one by applying _____-followed by-_____ pulses to detect intra-clock-domain delay faults.

Drawbacks:

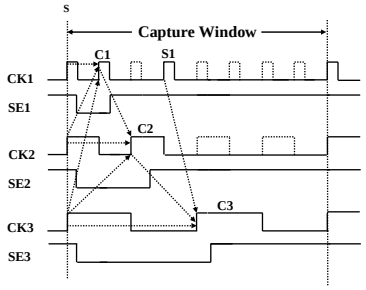
(1) Cannot detect ____-clock-domain delay faults
(2) Test time is long
(3) Single and global scan enable (GSE) signal can no longer be used



5.7 BIST Timing Control – Aligned Skewed-Load



Capture aligned skewed-load



Launch aligned skewed-load

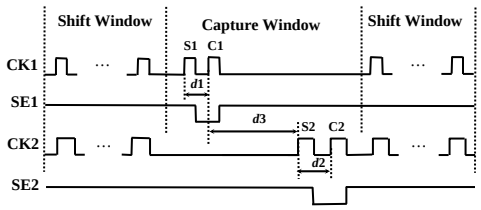
Benefits: Solve the long test time problem, Test all ____-clock-domain and _____-clock-domain faults

Drawbacks: Need _____ timing-control

5.7 BIST Timing Control – Staggered Skewed-Load

When two test clocks cannot be _____ precisely, we can simply insert a proper _____ to eliminate the clock skew. The last ____ pulse is used to create a transition and the output responses are caught by the next _____ pulse for each clock domain. This works for _____ clock domains.

Drawback: Need at-speed ____ _____ signal for each clock domain



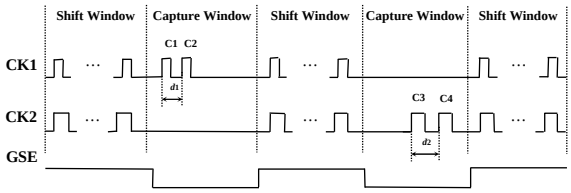
5.7 BIST Timing Control – Double Capture

- Solve the _____ _____ difficulty using skewed-load
- True at-speed test
- Double-capture benefits
  - Detect intra-clock-domain faults and inter-clock-domain _____ faults or _____ faults at-speed
  - Facilitate physical implementation
  - Ease _____ with ATPG

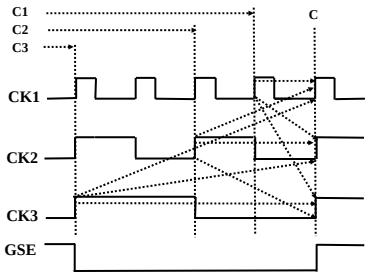
5.7 BIST Timing Control – One-Hot Double Capture

Test all clock domains one by one by applying ____ _____ capture pulses at their respective domains' _____ to test intra-clock-domain delay faults.

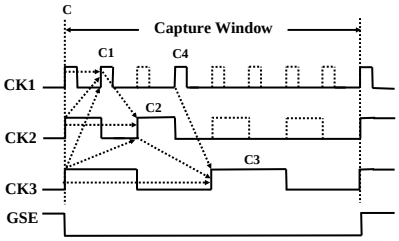
Benefit: true at-speed testing of _____-clock-domain _____ faults
Drawbacks: (1) Cannot detect _____-clock-domain delay faults
(2) Test time is long



5.7 BIST Timing Control – Aligned Double-Capture



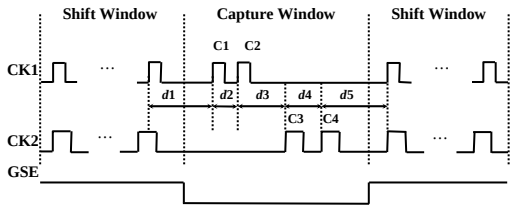
Aligned double-capture - I



Aligned double-capture - II

5.7 BIST Timing Control – Staggered Double-Capture

In the capture window, two capture pulses are generated for each clock domain. The first two capture pulses are used to create _____ at the _____ of scan cells, and the output responses to the transitions are _____ by the next two capture pulses, respectively.



5.7 Fault Detection

Capture-clocking scheme	Intra-structural	Intra-delay	Inter-structural	Inter-delay	Sync. design	Async. design
One-hot single-capture	√	-	√	-	√	√
Staggered single-capture	√	-	√	√	√	√
One-hot skewed-load	√	√	√	-	√	√
Aligned skewed-load	√	√	√	√	√	-
Staggered skewed-load	√	√	√	√	√	√
One-hot double-capture	√	√	√	-	√	√
Aligned double-capture	√	√	√	√	√	-
Staggered double-capture	√	√	√	√	√	√

Note: A hybrid double-capture scheme using _____ double-capture and _____ double-capture seems to be the _____ scheme for true at-speed testing

5.8 A Design Practice

An example of designing a logic BIST system for testing a _____ _____ (core) comprising two clock domains using s38417 and s38584. The two clock domains are taken from the _____ benchmark circuits.

Clock Domain	*No. of PIs*	*No. of POs*	*No. of flip-flops*	*No. of gates*
CD1 (s38417)	28	106	1636	22179
CD2 (s38584)	12	278	1452	19253

Design statistics

5.8 A Design Practice – Design Flow

- BIST Rule _____ and Violation _____
- Logic BIST System Design
- RTL _____ _____
- Design Verification and _____ _____ Enhancement

5.8 A Design Practice – BIST Rule Checking and Violation Repair

All DFT rule violations of the ____ design rules and _____ design rules must be repaired. In addition, we should be aware of the following design parameters:

- The number of test clocks present in the design
- The number of set/reset clocks present in the design

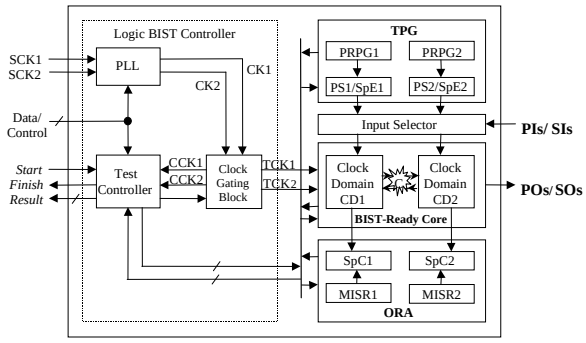
5.8 A Design Practice – Logic BIST System Design

The second step is to design the logic BIST system at the RTL, including:

- The type of logic BIST architecture to adopt
- The number of _____ (or _____) pairs to use
- The _____ of each _____ (or _____) pair
- The faults to be tested and BIST _____ _____ diagrams to be used
- The types of _____ _____ to be added

5.8 A Design Practice – Logic BIST Architecture

We choose to implement a _____-based architecture, since it is easy to integrate with scan/ATPG and is _____ used in industry.



A logic BIST system for testing a design with 2 cores

5.8 A Design Practice – TPG and ORA

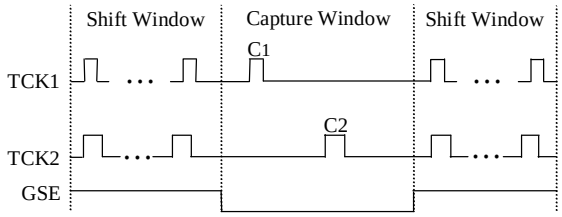
Next, we need to determine the _____ of each PRPG-MISR pair. Using a _____ PRPG-MISR pair for each clock domain allows us to _____ the _____ of each PRPG and MISR.

Clock Domain	*No. of scan chains*	*No. of shared SIs or SOs*	*Max. scan chain length*	*PRPG length*	*MISR length*
CD1 (s38417)	20	20	82	28	47
CD2 (s38584)	20	10	73	25	45

PRPG-MISR Choices

5.8 A Design Practice – Test Controller

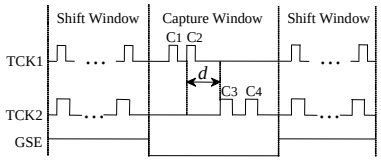
The test controller plays a central role in _____ the overall BIST operation. Often, external signals are controlled through an IEEE 1149.1 _____ Standard based test access port (TAP) controller. In order to test _____ faults in the BIST-ready core, we choose the staggered single-capture approach.



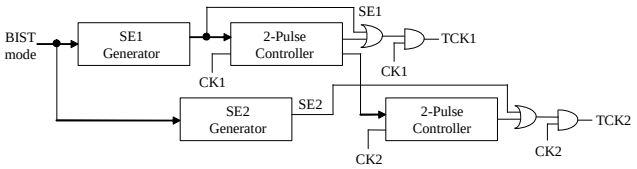
Slow-speed timing control using staggered single-capture

5.8 A Design Practice – Asynchronous Clocks

In order to test _____ faults in the BIST-ready core, we choose the staggered double-capture approach if CD1 and CD2 are asynchronous



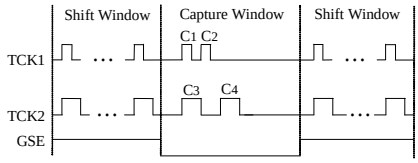
Staggered double-capture



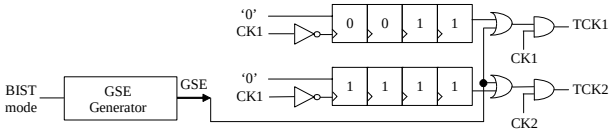
A daisy-chain clock-triggering circuit

5.8 A Design Practice – Synchronous Clocks

In order to test delay faults in the BIST-ready core, we choose the launch-aligned double-capture approach if CD1 and CD2 are synchronous



Launch aligned double-capture



A clock suppression circuit

5.8 A Design Practice – Re-Timing Logic

We recommend adding two pipelining registers between each _____ and the BIST-ready core, and two additional pipelining registers between the BIST-ready core and each _____. In this case, the maximum scan chain length for each clock domain, CD1 or CD2, is effectively increased by ___, not ___.

5.8 A Design Practice – Fault Coverage Enhancing Logic and Diagnostic Logic

In order to improve the circuit's fault coverage, we recommend adding _____ ____ _____ and additional logic for top-up ATPG support at the RTL. We also recommend including _____ _____ in the RTL BIST code to facilitate _____ and _____.

Test mode	*CD1 effective chain count*	*CD2 effective chain count*
Normal	0	0
BIST	20	20
ATPG	20	10
ATPG compression	20	20
Serial debug and diagnosis	1	1

Example test modes to be supported by the logic BIST system

5.8 A Design Practice – RTL BIST Synthesis

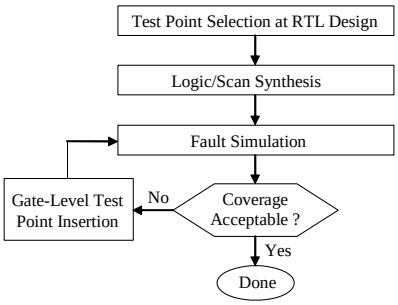
At this stage, it is possible to either _____ the logic BIST system __ _____ or generate the RTL code _____ using a (commercially available) RTL logic BIST tool.

In either case, the number of _____ _____ for each clock domain should be specified along with the _____ of their associated scan inputs (SIs) and scan outputs (SOs) without _____ the actual scan chains into the circuit.

5.8 A Design Practice – Design Verification and Fault Coverage Enhancement

Finally, the synthesized netlist needs to be verified with _____ and/or _____ verification.

Next, _____ _____ needs to be performed on the pseudo-random patterns generated by the TPG in order to determine the circuit's _____ _____.



Fault simulation and test point insertion flow