CPE 628
Chapter 3 – Logic and Fault Simulation

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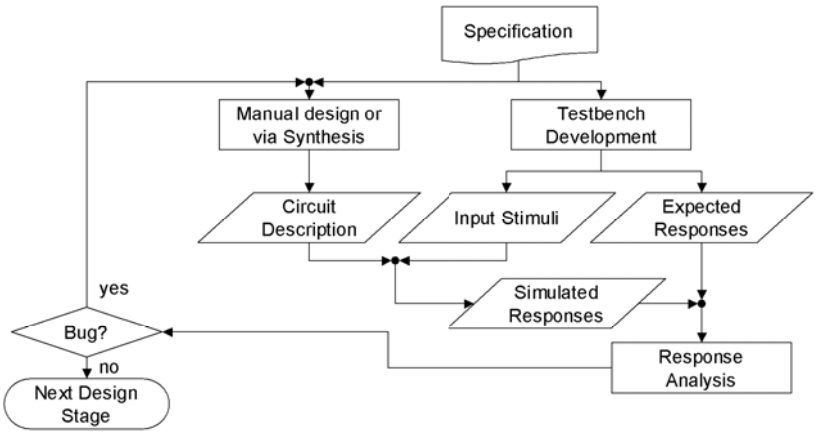
UAH

3.1 Introduction

- **Simulation is the process of _____ the behavior of a circuit design _____ it is physically built.**
- **_____ stage**
  - **_____ Simulation**
- **_____ development stage**
  - **_____ Simulation**

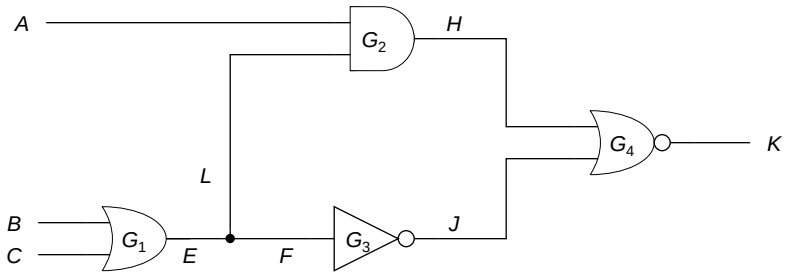
3.1 Introduction – Logic Simulation for Design Verification



3.1 Introduction – Fault Simulation for Test and Diagnosis

- **Fault simulation rates the _____ of a set of test patterns in detecting _____ defects expressed in fault _____, or fault _____.**
- **Fault simulation helps _____ _____ faults so that _____ _____ can be generated.**
- **In test _____, fault simulation identifies _____ test patterns.**

3.2 Simulation Models – Gate-Level Network



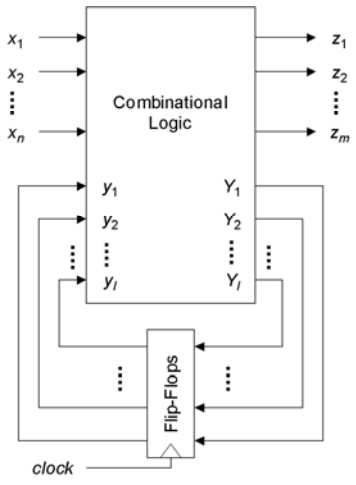
3.2 Simulation Models – Sequential Circuits

x_i: primary input (PI)

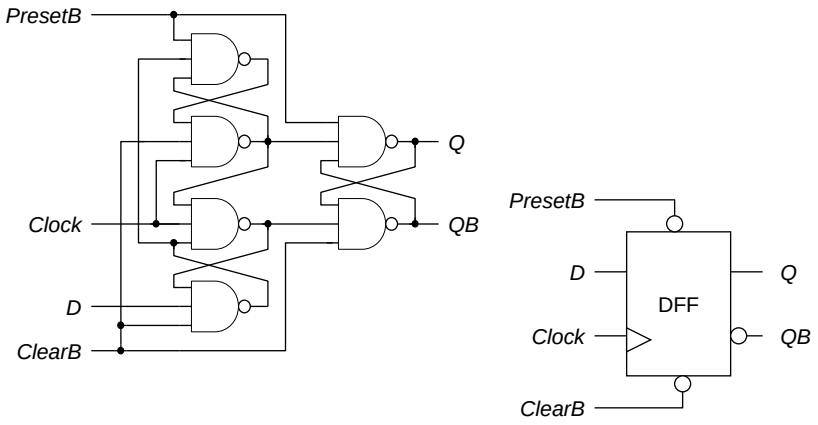
z_i: primary output (PO)

y_i: pseudo primary input (PPI)

Y_i: pseudo primary output (PPO)



3.2 Simulation Models – Sequential Circuits (Gate-Level Description)

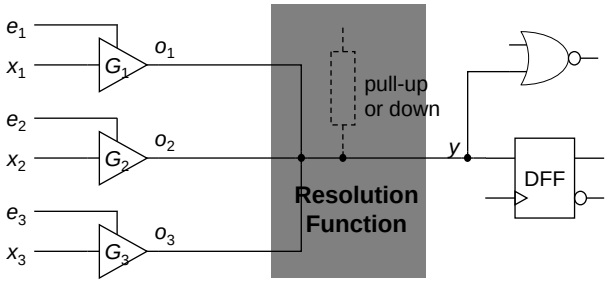


3.2 Simulation Models – Logic Symbols (0, 1, U, Z)

AND	0	1	*u*
0	0	0	0
1	0	1	*u*
u	0	*u*	*u*

OR	0	1	*u*
0	0	1	*u*
1	1	1	1
u	*u*	1	*u*

NOT	0	1	*u*
	1	0	*u*



3.2 Simulation Models – Bus Conflict

- Bus conflict occurs if at least ____ drivers drive the bus to _____ binary values
- To simulate _____ ___ behavior, one may insert a _____ _____ for each bus wire
  - May report only the _____ of bus conflict
  - May utilize _____ logic to represent _____ logic states (including logic _____ _____ and _____)

3.2 Simulation Model – Logical Element Evaluation

- _____ of evaluation _____ depends on
  - _____ logic symbols
  - _____ and _____ of logic elements
- Commonly used _____
  - _____
  - _____
  - _____
  - _____

3.2 Simulation Model – Logical Element Evaluation (Truth Table)

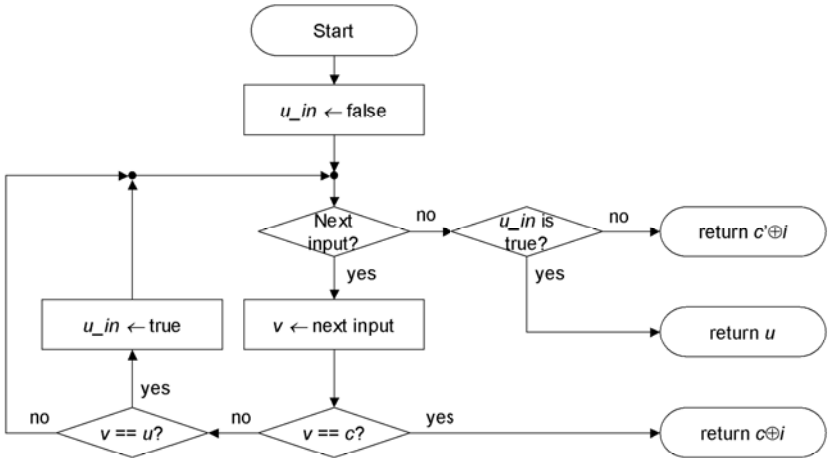
- The most _____ and easy to implement
  - For _____ logic, __ entries for *n*-input logic element
  - May use the input value as _____ _____
  - Table ____ increases _____ with the number of inputs
- Could be _____ for _____ logic
  - A _____ logic system requires a table of ___ entries for an *n*-input logic element

3.2 Simulation Model – Logical Element Evaluation (Input Scanning)

- The gate _____ can be determined by the _____ of inputs
  - If any of the inputs is the _____ value, the gate output is *c*⊕i, *where i is the* _____ *value*
  - Otherwise, if any of the inputs is ___, the gate output is ___
  - Otherwise, the gate output is _____

	c	*i*
AND	0	0
OR	1	0
NAND	0	1
NOR	1	1

3.2 Simulation Model – Logical Element Evaluation (Input Scanning)



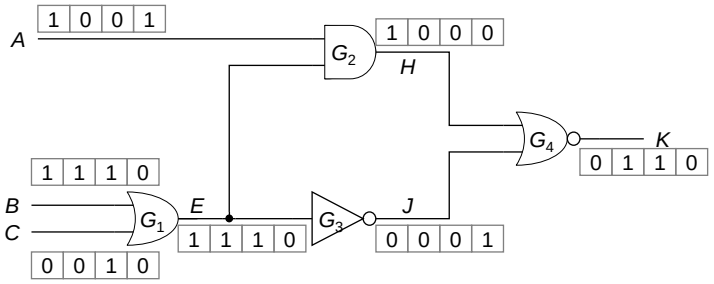
3.2 Simulation Model – Logical Element Evaluation (Input Counting)

- Keep the counts of _____ and _____ inputs
  - *c_count*: the number of _____ inputs
  - *u_count*: the number of _____ inputs
- _____ counts during logic _____
  - Example:

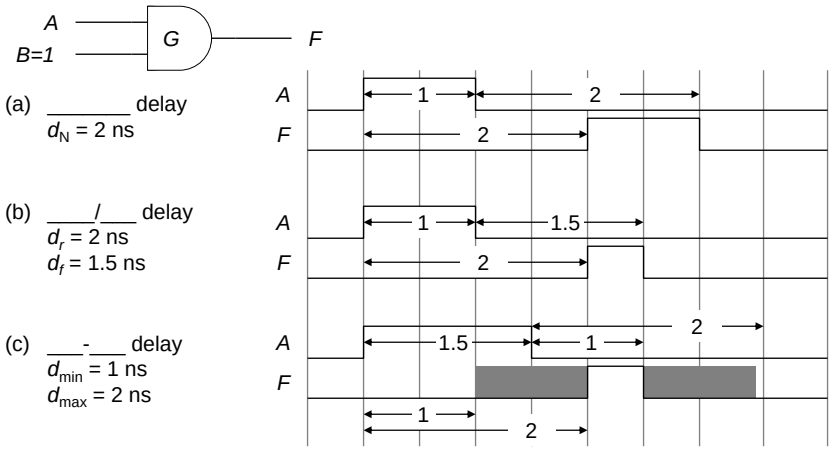
    One input of a _____ switches from __ to __
    - –*c_count* --
    - –*u_count* ++
- Same rules as _____ _____ used to evaluate gate outputs

3.2 Simulation Model – Logical Element Evaluation (Parallel Gate)

- Exploit the _____ _____ in the host computer
  - A __-bit computer can perform ___ logic operations in _____.

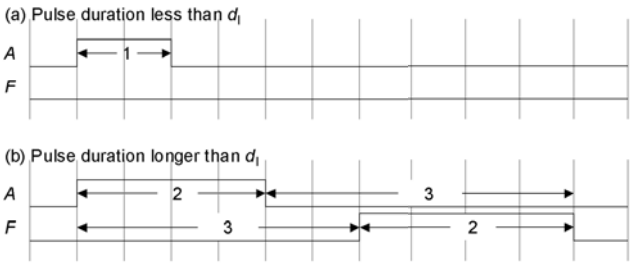


3.2 Simulation Model – Timing Models (Gate Delay)



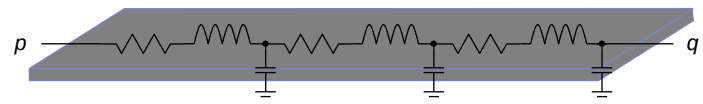
3.2 Simulation Model – Timing Models (Inertial Delay)

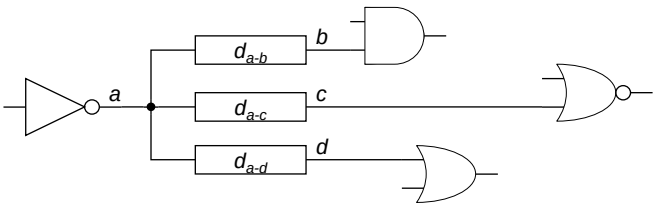
- The _____ input pulse _____ necessary for the output to _____ _____



3.2 Simulation Model – Timing Models (Wire Delay)

- Wires are inherently _____ and _____
- It takes ____ time for a signal to _____ along a wire





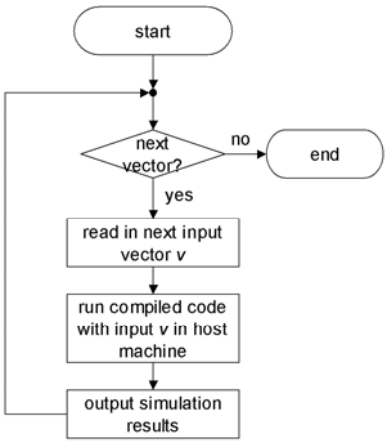
3.2 Simulation Model – Timing Models (Functional Element Delay)

- For more complicated _____ elements like _____

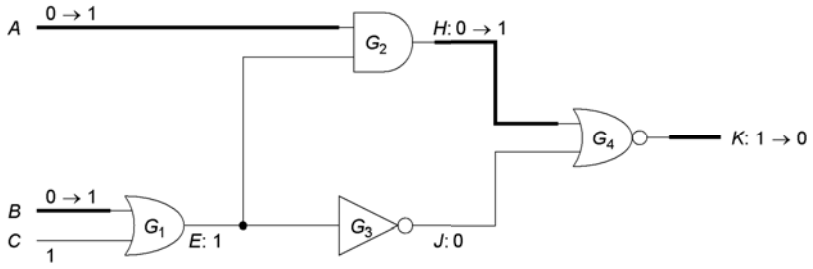
Input condition				Present state	Outputs		Delays (ns)		
D	*Clock*	*PresetB*	*ClearB*	*q*	*Q*	*QB*	to *Q*	to *QB*	Comments
X	*X*	↓	0	0	↑	↓	1.6	1.8	Asynchronous preset
X	*X*	0	↓	1	↓	↑	1.8	1.6	Asynchronous clear
1	↑	0	0	0	↑	↓	2	3	*Q*: 0→1
0	↑	0	0	1	↓	↑	3	2	*Q*: 1→0

3.3 Logic Simulation – Compiled-Code Simulation

- **Translate the logic network into a series of _____ _____ that model the _____ of the individual _____ and the _____ between them.**
- **_____ because the entire network must be executed for every _____ _____ though only a _____ _____ of it is _____**



3.3 Logic Simulation – Event-Driven Simulation



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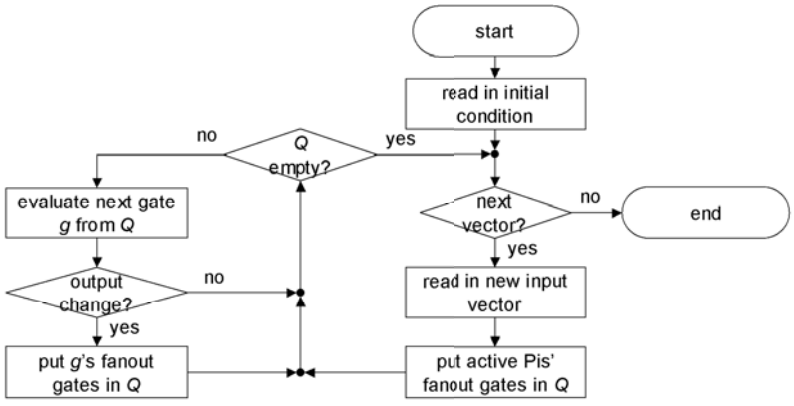
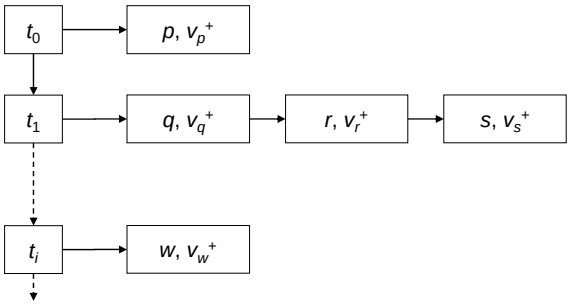


3.3 Logic Simulation – Event-Driven Simulation

- Need a _____ scheduler than the _____ _____
  - Not only _____ _____ but also _____ to evaluate



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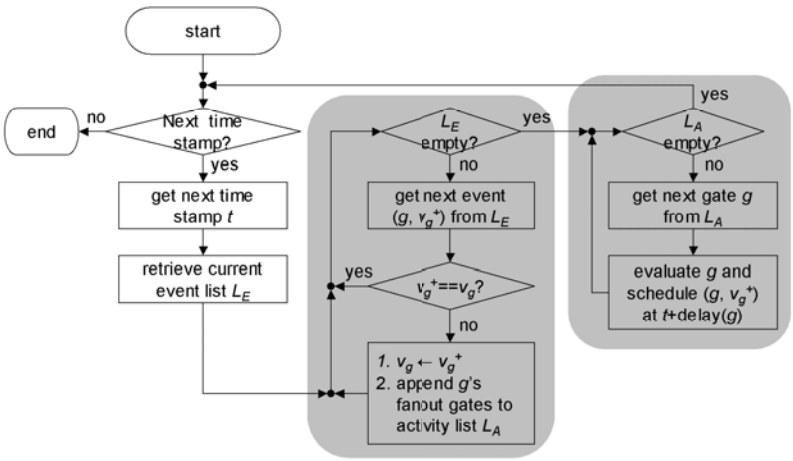

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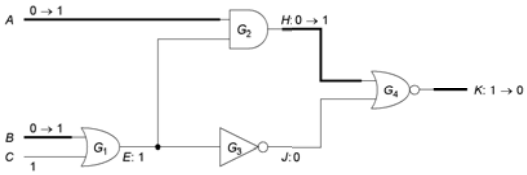
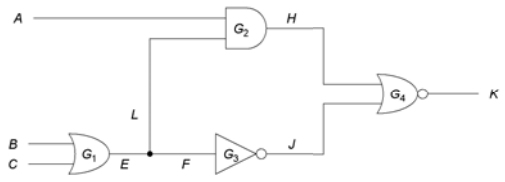


Delays
G1 – 8, G2 – 8, G3 – 4, G4 – 6
Events
(A, 1, 0), (C, 0, 2), (B, 0, 4), (A, 0, 8)

Time	L_E	L_A	Scheduled events

3.3 Logic Simulation – Hazards



Delays
G1 – 2, G2 – 2, G3 – 3, G4 – 2
Events
(A, 1, 0), (B, 1, 0), (C, 0, 0), (B, 0, 1)

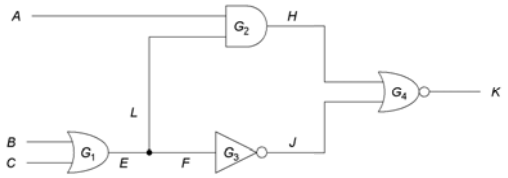
Types: Static 0-hazard, static 1-hazard, dynamic 0-hazard, dynamic 1-hazard

3.3 Logic Simulation – Hazards (Static Hazard Detection)

- Let $V^1 = v_1^1 v_2^1 \cdots v_n^1$ and $V^2 = v_1^2 v_2^2 \cdots v_n^2$ be _____ consecutive _____ _____
- Add a ___ _____ $V^+ = v_1^+ v_2^+ \cdots v_n^+$ according to the following rule

$$v_i^+ = \begin{cases} v_i^1 & \text{if } v_i^1 = v_i^2 \\ u & \text{if } v_i^1 \neq v_i^2 \end{cases}$$

- _____ the $V^1V^+V^2$ sequence using _____ logic
- Any signal that is 1*u*1 or 0*u*0 indicates the _____ of a _____ hazard.



3.4 Fault Simulation – Introduction

Given

– _____, _____, _____

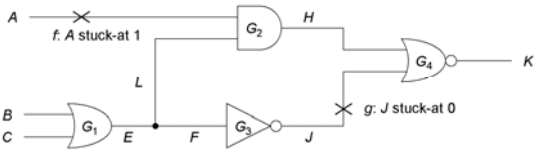
Determine

– _____, _____, _____

- Task _____ to
  - *n*: Circuit ____, _____ of logic gates
  - *p*: Number of ____ _____
  - *f* : Number of _____ _____
- Since *f* is _____ _____ to *n*, the overall time _____ is $O(pn^2)$

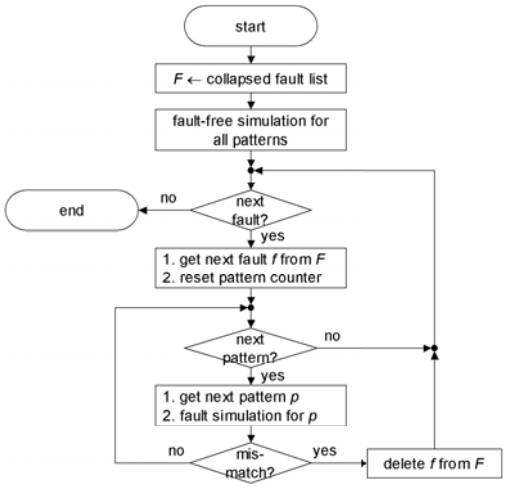
3.4 Fault Simulation – Serial Fault Simulation

- First, perform _____ logic simulation on the _____ circuit, obtain Good (_____) response
- For ____ _____, perform _____ _____ and logic simulation, obtain _____ circuit response



Pat. #	Input			Internal					Output		
	A	B	C	E	F	L	J	H	K_{good}	K_f	K_g
P1	0	1	0	1	1	1	0	0	1	0	1
P2	0	0	1	1	1	1	0	0	1	0	1
P3	1	0	0	0	0	0	1	0	0	0	1

3.4 Fault Simulation – Serial Fault Simulation



3.4 Fault Simulation – Serial Fault Simulation(Fault Dropping)

- _____ simulation of the _____ fault
- Example
  - Suppose we are to simulate P_1, P_2, P_3 in order
  - Fault _ is detected by ___
  - Do not simulate _ for ___, ___
- For fault _____
  - Most faults are detected after _____ ___ test patterns have been applied
- For fault _____
  - _____ to obtain the _____ fault simulation _____

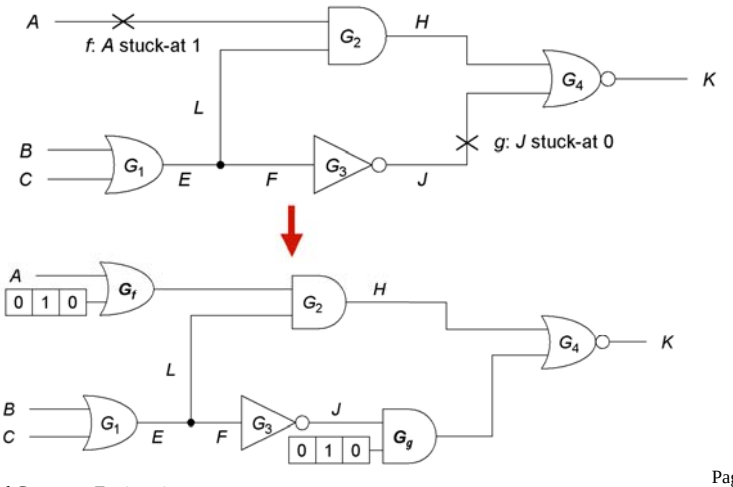
3.4 Fault Simulation – Serial Fault Simulation(Pros and Cons)

- Advantages
  - Easy to _____
  - Ability to handle a ____ _____ of fault models
- Disadvantages
  - ____ ____

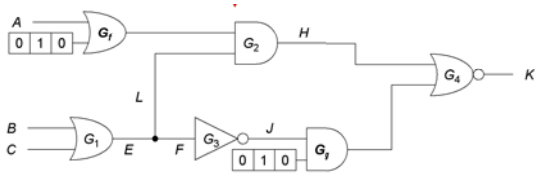
3.4 Fault Simulation – Parallel Fault Simulation

- Exploit the _____ parallelism of _____ operations
- _____ fault simulation
  - Parallel in _____
- _____ _____ fault simulation
  - Parallel in _____
- Assumption
  - Use _____ logic: ____ ___ is enough to store logic _____
  - Use __-bit wide ____ word
- Parallel simulation
  - ____ bits for faulty circuits
  - __ bit for fault-free circuit
- Process _____ and _____ circuit in parallel using bitwise logic operations

3.4 Fault Simulation – Parallel Fault Simulation(Parallel Faults Fault Injection)



3.4 Fault Simulation – Parallel Fault Simulation(Parallel Faults Example)



Pat #		Input				Internal						Output
		A	A_f	B	C	E	F	L	J	J_g	H	K
P_1	FF	0	0	1	0	1	1	1	0	0	0	1
	f	0	1	1	0	1	1	1	0	0	1	0
	g	0	0	1	0	1	1	1	0	0	0	1
P_2	FF	0	0	0	1	1	1	1	0	0	0	1
	f	0	1	0	1	1	1	1	0	0	1	0
	g	0	0	0	1	1	1	1	0	0	0	1
P_3	FF	1	1	0	0	0	0	0	1	1	0	0
	f	1	1	0	0	0	0	0	1	1	0	0
	g	1	1	0	0	0	0	0	1	0	0	1

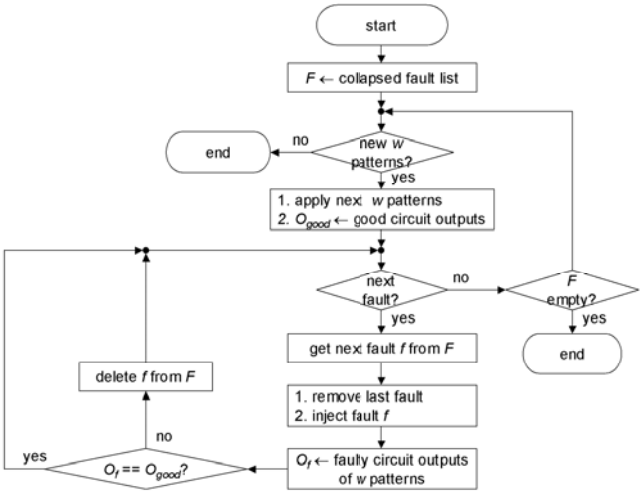
3.4 Fault Simulation – Parallel Fault Simulation(Parallel Faults Pros and Cons)

- Advantages
  - A _____ number of faults are detected by _____ _____ when simulating the _____ of test sequence
- Disadvantages
  - Only applicable to the ____ or _____ _____ models
  - Faults cannot be _____ unless all _____ faults are detected

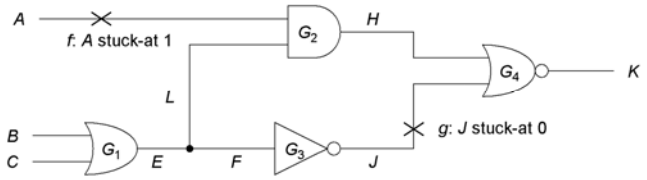
3.4 Fault Simulation – Parallel Fault Simulation(Parallel Patterns)

- Parallel pattern single fault propagation (PPSFP)
- Parallel _____
  - With a ____ data width, __ _____ _____ are packed into a word and simulated for the _____ or _____ circuit
- Single _____
  - First, _____ simulation
  - Next, for each _____, fault _____ and _____ _____ simulation

3.4 Fault Simulation – Parallel Fault Simulation(Parallel Patterns Algorithm)



3.4 Fault Simulation – Parallel Fault Simulation(Parallel Patterns Example)



		Input			Internal					Output
		A	B	C	E	F	L	J	H	K
Fault Free	P_1	0	1	0	1	1	1	0	0	1
	P_2	0	0	1	1	1	1	0	0	1
	P_3	1	0	0	0	0	0	1	0	0
f	P_1	1	1	0	1	1	1	0	1	0
	P_2	1	0	1	1	1	1	0	1	0
	P_3	1	0	0	0	0	0	1	0	0
g	P_1	0	1	0	1	1	1	0	0	1
	P_2	0	0	1	1	1	1	0	0	1
	P_3	1	0	0	0	0	0	0	0	1

3.4 Fault Simulation – Parallel Fault Simulation(Parallel Patterns Pros and Cons)

- Advantages
  - Fault is _____ as soon as _____
  - Best for simulating _____ _____ that come later, where _____ _____ _____ per _____ is lower
- Disadvantages
  - Not suitable for _____ circuits

3.4 Fault Simulation – Deductive Fault Simulation

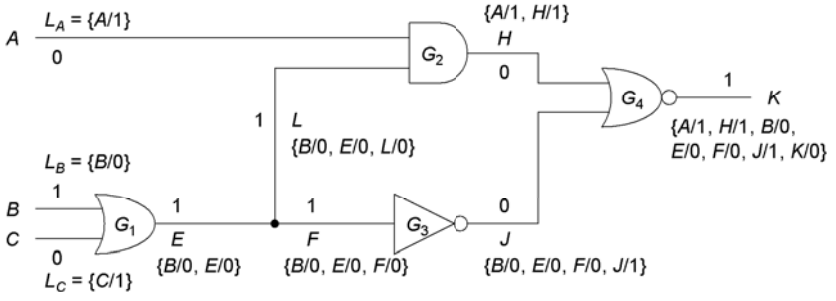
- Based on _____ _____ rather than _____
- Fault ___ attached to _____ __ denoted as __
  - Set of _____ causing __ to differ from its _____ value
- Fault ____ _____
  - _____ the fault ____ of a gate _____ from those of the gate _____ based on logic reasoning

3.4 Fault Simulation – Deductive Fault Simulation(Example Pattern 1)

- All gate inputs hold _____ value

$$L_z = \left(\bigcup_{j \in I} L_j \right) \cup \{ z/(c \oplus i) \}$$

c : _____ value
i : _____ value
I : set of gate _____
z : gate _____
S : _____ holding _____ value

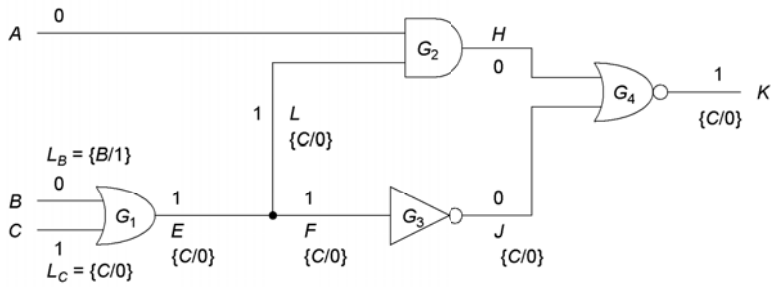


3.4 Fault Simulation – Deductive Fault Simulation(Example Pattern 2)

- All gate inputs hold non-controlling value

$$L_z = \left(\bigcup_{j \in I} L_j \right) \cup \{ z/(c \oplus i) \}$$

c : controlling value
i : inversion value
I : set of gate inputs
z : gate output
S : inputs holding controlling value

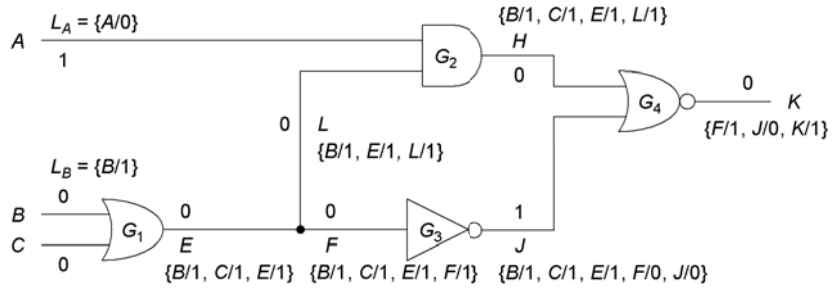


3.4 Fault Simulation – Deductive Fault Simulation(Example Pattern 3)

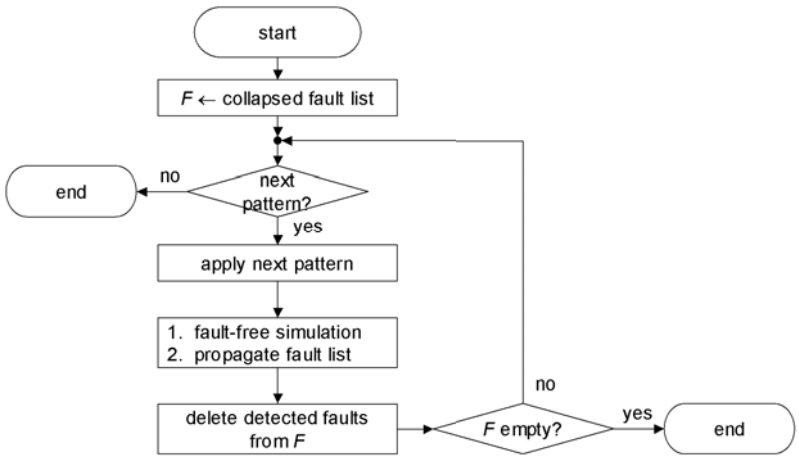
- At least ____ input holds _____ value

$$L_z = [(\bigcap_{j \in S} L_j) - (\bigcup_{j \in I-S} L_j)] \cup \{ z/c \oplus i' \}$$

c : controlling value
i : inversion value
I : set of gate inputs
z : gate output
S : inputs holding controlling value



3.4 Fault Simulation – Deductive Fault Simulation(Algorithm)



3.4 Fault Simulation – Deductive Fault Simulation(Pros and Cons)

- Advantages
  - Very _____
  - Simulate ____ faults in ___ ____
- Disadvantages
  - Not easy to handle _____
  - Only for _____ timing model
  - Potential _____ _____ problem

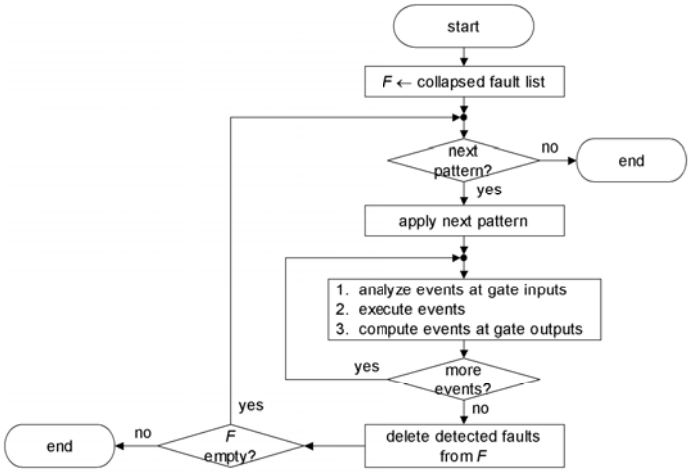
3.4 Fault Simulation – Concurrent Fault Simulation

- Simulate only _____ parts of whole circuit
- _____ _____ simulation with ____-___ and _____ circuits simulated altogether
- Concurrent ____ ___ for each gate
  - Consist of a set of _____ gates
    - –Fault _____ & associated gate ___ values
  - _____ only contains _____ faults
  - Fault _____ from previous stage

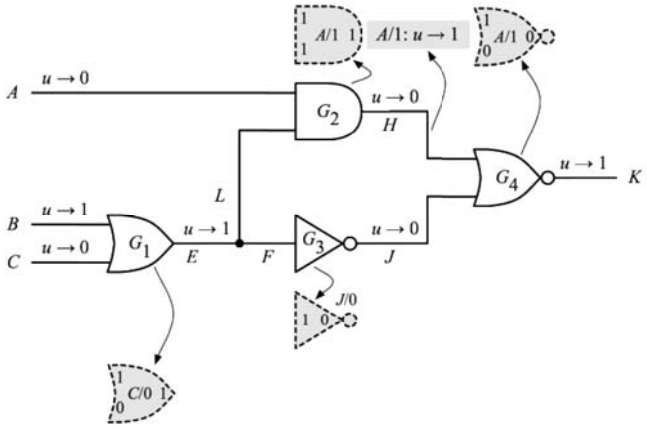
3.4 Fault Simulation – Concurrent Fault Simulation(Definitions)

- ____ event
  - Events that happen in ____ circuit
  - Affect both _____ gates and ___ gates
- ____ event
  - Events that occur in the _____ circuit of corresponding fault
  - Affect ____ ___ gates
- _____
  - _____ of new bad gates
- _____
  - _____ of bad gates whose ___ _____ are the ____ as _____ good gates

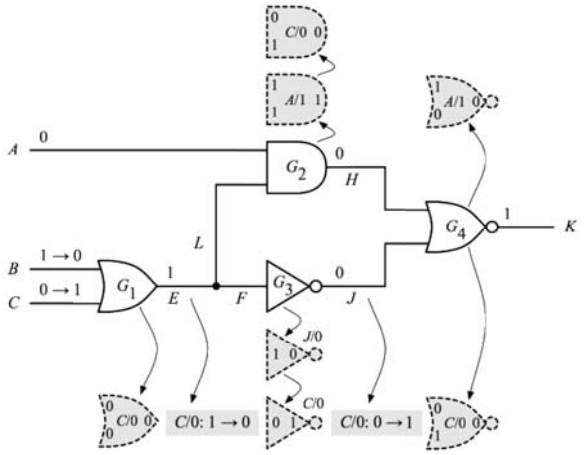
3.4 Fault Simulation – Concurrent Fault Simulation(Algorithm)



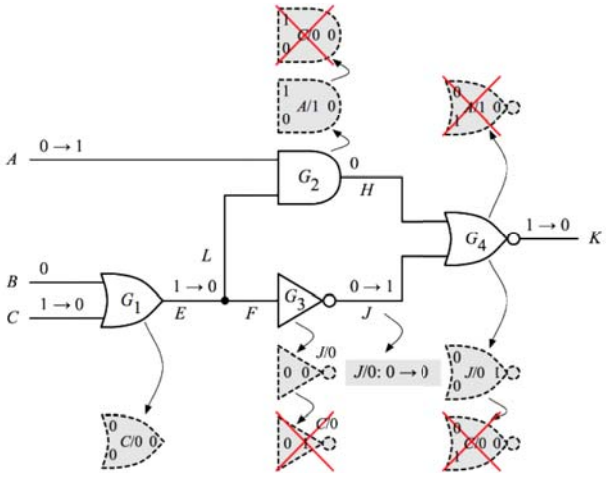
3.4 Fault Simulation – Concurrent Fault Simulation(Example 1)



3.4 Fault Simulation – Concurrent Fault Simulation(Example 2)



3.4 Fault Simulation – Concurrent Fault Simulation(Example 3)



3.4 Fault Simulation – Concurrent Fault Simulation(Pros and Cons)

- Advantages
  - _____
- Disadvantages
  - Potential _____ problem
    - –Size of the _____ ____ ____ changes at ___ ____

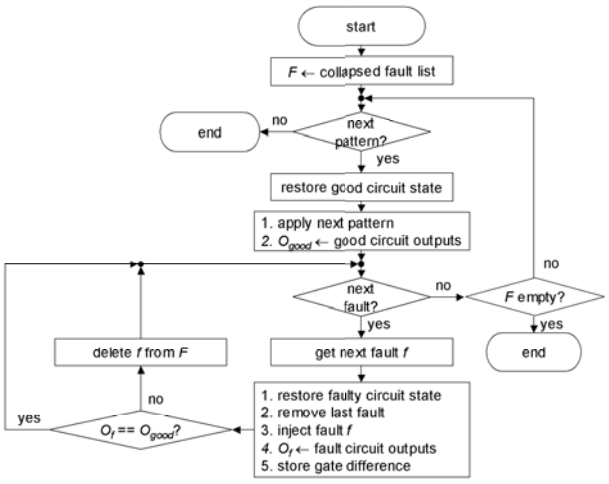
3.4 Fault Simulation – Differential Fault Simulation

- _____ the _____ of two techniques
  - _____ fault simulation
  - _____
- Idea
  - Simulate __ ____ every faulty circuit
  - Track only _____ between _____ circuit and ____ _____ one
  - Inject _____ as _____
  - Easily implemented by _____-_____ simulator

3.4 Fault Simulation – Differential Fault Simulation(Sequence)

	P_1	P_2	…	P_i	P_{i+1}	…	P_n
Good	G_1	G_2	…	G_i	G_{i+1}	…	G_n
f_1	$F_{1,1}$	$F_{1,2}$	…	$F_{1,i}$	$F_{1,i+1}$	…	$F_{1,n}$
f_2	$F_{2,1}$	$F_{2,2}$	…	$F_{2,i}$	$F_{2,i+1}$	…	$F_{2,n}$
.	.	.	…	.	.	…	.
f_k	$F_{k,1}$	$F_{k,2}$	…	$F_{k,i}$	$F_{k,i+1}$	…	$F_{k,n}$
f_{k+1}	$F_{k+1,1}$	$F_{k+1,2}$	…	$F_{k+1,i}$	$F_{k+1,i+1}$	…	$F_{k+1,n}$
.	.	.	…	.	.	…	.
f_m	$F_{m,1}$	$F_{m,2}$	…	$F_{m,i}$	$F_{m,i+1}$	…	$F_{m,n}$

3.4 Fault Simulation – Differential Fault Simulation(Algorithm)



3.4 Fault Simulation – Differential Fault Simulation(Pros and Cons)

Advantages

- Suitable for _____ fault simulation

Disadvantages

- Including _____ information makes the _____ _____ problem explode

3.4 Fault Simulation – Fault Detection Decision

- _____ detected fault
  - Outputs of fault-free and faulty circuit are _____
    - –1/0 or 0/1
    - –No unknowns, no *Z*
- _____ detected fault
  - Whether the fault is detected is _____
  - Example: stuck-at-0 on _____ signal of tri-state buffer
- _____ faults
  - Cause circuit to _____
  - Impossible to _____ faulty circuit _____
- _____ faults
  - Catastrophic fault effect
  - Example: stuck-at fault on _____
  - Usually counted as _____

3.4 Fault Simulation – Comparison of Techniques

- _____
  - _____ fault simulation: _____
  - _____ fault simulation: O(n^3), n: num of _____
  - _____ fault simulation: O(n^2)
  - _____ fault is faster than _____ fault simulation
  - _____ fault simulation: even faster than _____ fault simulation and _____
- _____ usage
  - _____ fault simulation, _____ fault simulation: no problem
  - _____ fault simulation: _____ memory _____, hard to _____ size
  - _____ fault simulation: more _____ than _____ fault simulation
  - _____ fault simulation: less memory problem than _____ fault simulation

3.4 Fault Simulation – Comparison of Techniques

- _____-_____ fault simulation to handle unknown (X) and/or high-impedance (Z)
  - _____ fault simulation, _____ fault simulation, _____ fault simulation: easy to handle
  - _____ fault simulation: difficult
- _____ and _____ modeling capability
  - _____ fault simulation: no problem
  - _____ fault simulation, deductive fault simulation: not capable
  - _____ fault simulation: capable
  - _____ fault simulation: capable

3.4 Fault Simulation – Comparison of Techniques

- _____ circuit
  - _____ fault simulation, _____ fault simulation, _____ fault simulation, _____ fault simulation: no problem
  - _____: difficult
  - _____ fault simulation: difficult due to many _____

3.4 Fault Simulation – Comparison of Techniques

- _____ and _____ fault simulation are popular for combinational (_____) circuits
- _____ fault simulation and _____ fault simulation is popular for _____ circuits
- _____-____ fault simulation
  - Prevent memory _____ problem
- _____ fault simulation
  - Reduce fault simulation ____

3.5 Concluding Remarks

- Fault simulation is very important for
  - _____
  - _____
  - _____ _____
- Popular techniques
  - _____, _____, _____, _____, _____
- Requirements for fault simulation
  - ____ speed, _____ memory usage, modeling _____ blocks, _____ circuits