CPE 628
Chapter 2 – Design for Testability

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UAH

2.1 Introduction

- **Difficulties in _____________ and __________ the _________ states of sequential circuits led to providing direct ____________ access for storage elements.**
- **____ ______, whereby selected storage elements are connected into a ____ _____, is currently the most popular ___________ DFT approach.**
- **Scan can be ____ or ______, ____ more prominent now.**
- **Scan is now the basis for _______ _______ (BIST) techniques.**
- **Recently, DFT is migrating from ____ to ________ _________ level.**

2.2 Testability Analysis

- Test ___________ programs use ____________ ________ to aid in making decisions.
- Types of testability analysis
  - _______________
  - ______________
  - _______________
  - ___________________

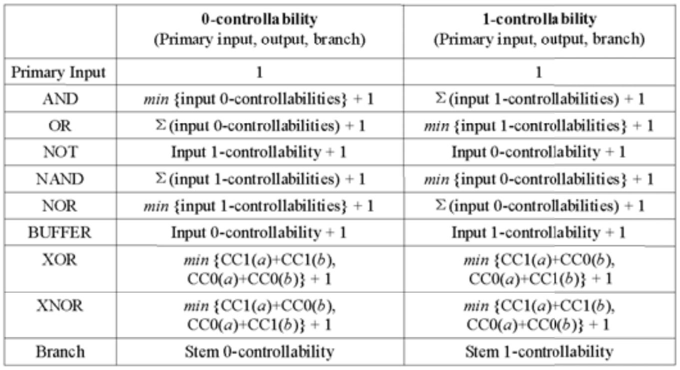
2.2 Testability Analysis – SCOAP

- For each ______ __ in a logic circuit, the following values are calculated.
  - CC0(s) – combinational ______________ of s
  - CC1(s) – combinational ______________ of s
  - CO(s) – combinational ____________ of s
  - SC0(s) – sequential _______________ of s
  - SC1(s) – sequential _______________ of s
  - SO(s) – sequential ___________ of s
- CC0 = CC1 = __ for a _______ _____
- SC0 = SC1 = __ for a _______ ______
- CO = SO = __0 for a _______ _______

2.2 Testability Analysis –

SCOAP (Combinational Calculations)

- **Assign _____ order for each _____.**
- **Calculate _____________ for all signals starting with ________ ______(___), proceeding in ______ order (_______ _____)**

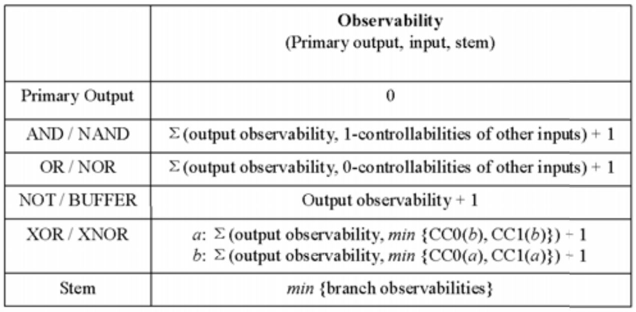


	0-controllability (Primary input, output, branch)	1-controllability (Primary input, output, branch)
Primary Input	1	1
AND	*min* {input 0-controllabilities} + 1	Σ(input 1-controllabilities) + 1
OR	Σ(input 0-controllabilities) + 1	*min* {input 1-controllabilities} + 1
NOT	Input 1-controllability + 1	Input 0-controllability + 1
NAND	Σ(input 1-controllabilities) + 1	*min* {input 0-controllabilities} + 1
NOR	*min* {input 1-controllabilities} + 1	Σ(input 0-controllabilities) + 1
BUFFER	Input 0-controllability + 1	Input 1-controllability + 1
XOR	*min* {CC1(*a*)+CC1(*b*), CC0(*a*)+CC0(*b*)} + 1	*min* {CC1(*a*)+CC0(*b*), CC0(*a*)+CC1(*b*)} + 1
XNOR	*min* {CC1(*a*)+CC0(*b*), CC0(*a*)+CC1(*b*)} + 1	*min* {CC1(*a*)+CC1(*b*), CC0(*a*)+CC0(*b*)} + 1
Branch	Stem 0-controllability	Stem 1-controllability

2.2 Testability Analysis –

SCOAP (Combinational Calculations)

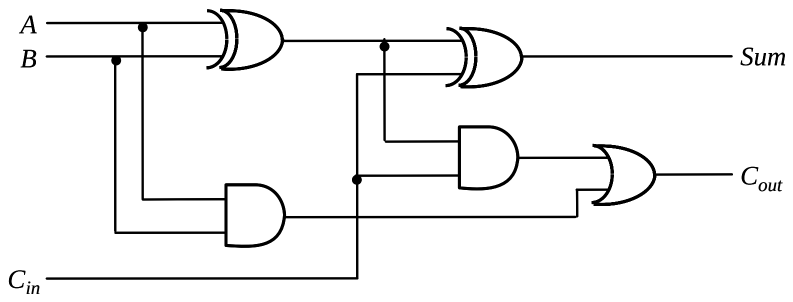
- **Starting from _________ ________, calculate __________________.**



	Observability (Primary output, input, stem)
Primary Output	0
AND / NAND	Σ(output observability, 1-controllabilities of other inputs) + 1
OR / NOR	Σ(output observability, 0-controllabilities of other inputs) + 1
NOT / BUFFER	Output observability + 1
XOR / XNOR	*a*: Σ(output observability, *min* {CC0(*b*), CC1(*b*)}) + 1 *b*: Σ(output observability, *min* {CC0(*a*), CC1(*a*)}) + 1
Stem	*min* {branch observabilities}

2.2 Testability Analysis –

SCOAP (Combinational Calculations)



2.2 Testability Analysis –

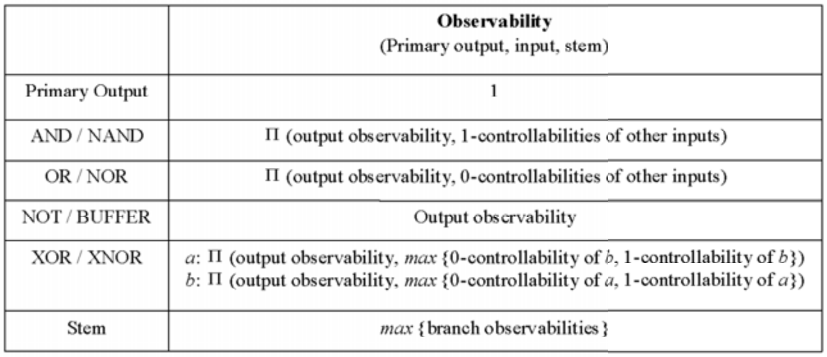
Probability-Based

- **For each signal s in a combinational circuit, calculate**
  - **CO(s) – ______________-_____ 0-controllability of s**
  - **C1(s) – ______________-____ 1-controllability of s**
  - **O(s) – ____________-_____ observability of s**
- **C0(s) and C1(s) are the probabilities of controlling s to 0 and 1 from primary inputs, respectively.**
- **O(s) is the probability of observing signal s at ___________ outputs.**
- **C0 = C1 = ___ for a PI**
- **_______ + ______ = ___**

2.2 Testability Analysis – Probability-Based (Controllability Calculation Rules)

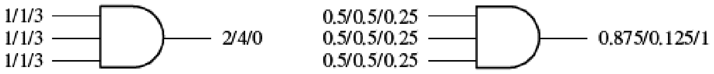
	0-controllability (Primary input, output, branch)	**1-controllability** (Primary input, output, branch)
Primary Input	p_0	$p_1 = 1 - p_0$
AND	1 – (output 1-controllability)	Π (input 1-controllabilities)
OR	Π (input 0-controllabilities)	1 – (output 0-controllability)
NOT	Input 1-controllability	Input 0-controllability
NAND	Π (input 1-controllabilities)	1 – (output 0-controllability)
NOR	1 – (output 1-controllability)	Π (input 0-controllabilities)
BUFFER	Input 0-controllability	Input 1-controllability
XOR	1 – 1-controllabilty	$\Sigma(\mathrm{C1}(a) \times \mathrm{C0}(b), \mathrm{C0}(a) \times \mathrm{C1}(b))$
XNOR	1 – 1-controllability	$\Sigma(\mathrm{C0}(a) \times \mathrm{C0}(b), \mathrm{C1}(a) \times \mathrm{C1}(b))$
Branch	Stem 0-controllability	Stem 1-controllability

2.2 Testability Analysis – Probability-Based (Observability Calculation Rules)



	Observability (Primary output, input, stem)
Primary Output	1
AND / NAND	Π (output observability, 1-controllabilities of other inputs)
OR / NOR	Π (output observability, 0-controllabilities of other inputs)
NOT / BUFFER	Output observability
XOR / XNOR	a: Π (output observability, *max* {0-controllability of b, 1-controllability of b}) b: Π (output observability, *max* {0-controllability of a, 1-controllability of a})
Stem	*max* {branch observabilities}

2.2 Testability Analysis – Probability-Based (Comparison to SCOAP)



(a) SCOAP combinational measures (b) Probability-based measures

Signals with _____ probability-based testability measures tend to be difficult to test with _________ or ________________ test patterns.

The faults on these lines are often referred to as ______-_______ ___________.

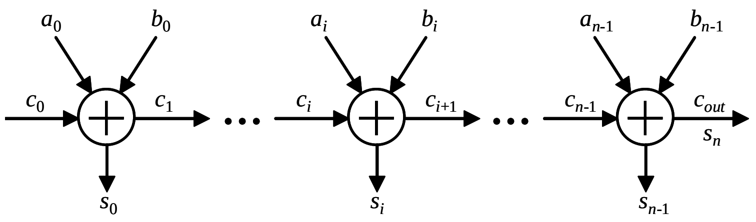
2.2 Testability Analysis – Simulation-Based

- **Simulation-based methods use ______ ___________ for testability analysis and can be used as an ______________ to or a ________________ to ___________-based analysis.**
- **A sample set of input test patterns are selected that are either generated _____________ or derived from a ________ __________ ___.**
- **______ _____________ is conducted to collect the ____________ of all or part of signal lines of interest**
  - **Occurrences of ___, ___**
  - **Occurrences of ___, ____ transitions**
- **Due to long run times, this technique is used mostly for ____- or ______-_______ applications.**

2.2 Testability Analysis – RTL

- Improve ____ ____ testability
- Improve the ______ _____ testability of a ____-_____ logic BIST circuit
- Lead to more _______ results
  - –The number of ____________ _______ is much less
- Become more time _________
  - –Much ________ than an equivalent ____-level model

2.2 Testability Analysis – RTL(Example)



Ripple Carry Adder

2.2 Testability Analysis – RTL(Example-1-Controllability)

The probability-based 1-controllability measures of *s*s_i and c_i+1, denoted by C1(s_i) and C1(c_i+1), are calculated as follows:

$$C1(s_i) = \alpha + C1(c_i) - 2 \times (\alpha \times C1(c_i))$$
$$C1(c_i + 1) = \alpha \times C1(c_i) + C1(a_i) \times C1(b_i)$$

$$\alpha = C1(a_i) + C1(b_i) - 2 \times C1(a_i) \times C1(b_i)$$

α is the probability that $(a_i \oplus b_i) = 1$

$C1(s_i)$ is the probability that $(a_i \oplus b_i \oplus c_i) = 1$

2.2 Testability Analysis – RTL(Example-0-Controllability & Observability)

- **The probability-based 0-controllability of each output *l*, denoted by C0(*l*), in the *n*-bit ripple-carry adder is ________.**

O(*l*, s_i) is defined as the probability that a signal change on *l* will result in a signal change on s_i.

Since

$$O(a_i, s_i) = O(b_i, s_i) = O(c_i, s_i) = O(s_i)$$
$$\text{where } i = 0, 1, \ldots, n-1$$

Harder for _____

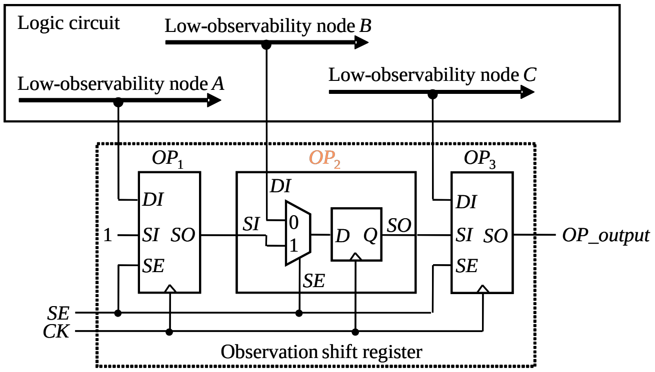
2.3 Design for Testability Basics

- __ ___ DFT (literally ____ _____)
  - Effects are _____ and not _____________
  - Not __________
  - Difficult to ________
- A __________ DFT
  - Easily _____________ and _______
  - Yields the __________ results
  - Easy to _____________

2.3 Design for Testability Basics –
Ad Hoc Approach

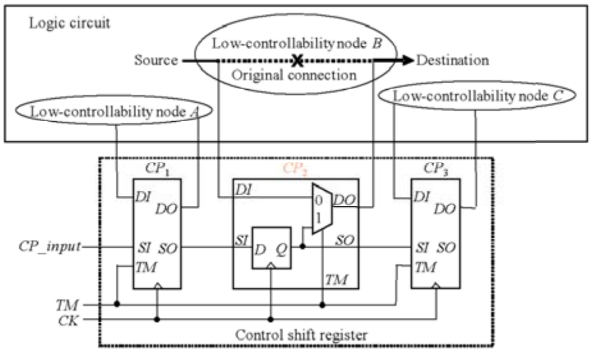
- **Typical Ad Hoc DFT techniques**
  - **Insert _____ points**
  - **Avoid ______________ ________ for storage elements**
  - **Avoid combinational ________ _____**
  - **Avoid ___________ logic**
  - **Avoid _____________ logic**
  - **__________ a large circuit into _____ ______**

2.3 Design for Testability Basics – Ad Hoc Techniques(Observability Test Points)



OP2 shows the structure of an ___________________, which is composed of a multiplexer (MUX) and a D flip-flop.

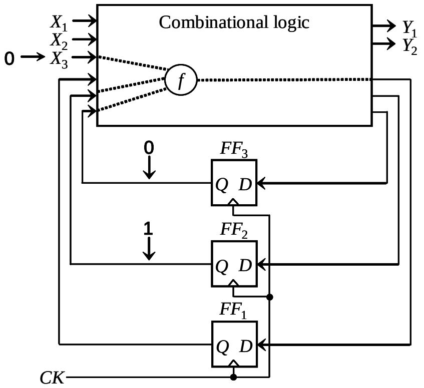
2.3 Design for Testability Basics – Ad Hoc Techniques(Controllability Test Points)



A MUX is inserted between the source and destination ends. During normal operation, TM = 0, such that the value from the source end drives the destination end through the 0 port of the MUX.

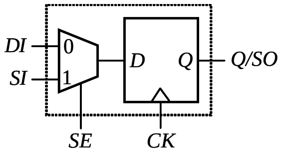
During test, TM = 1 such that the value from the D flip-flop drives the destination end through the 1 port of the MUX.

2.3 Design for Testability Basics – Structured Approach

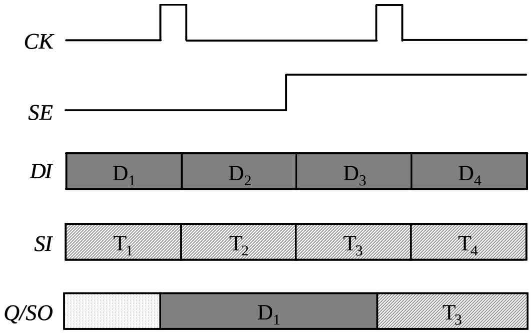


- •To detect a fault, f
  - •Shift ___ the desired _____ _________
  - •Apply desired values on _________ _______
  - •Apply one ______ ______ and ________ fault effect
  - •Shift _____ ___________ (shift in next test stimulus for ______________)

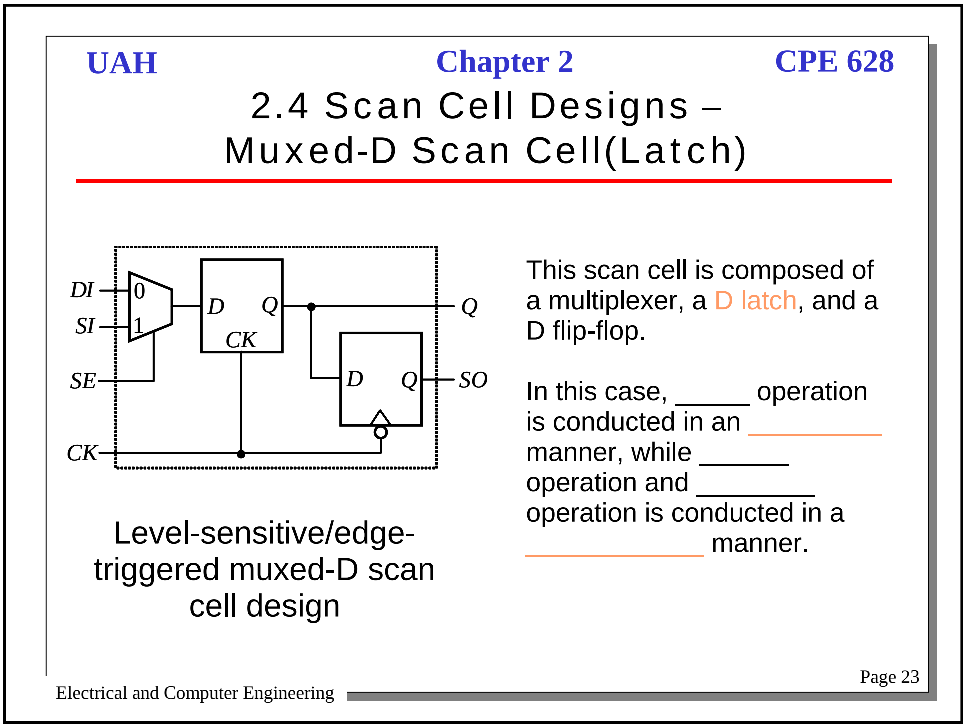
2.4 Scan Cell Designs – Muxed-D Scan Cell(Flip-Flop)



Edge-triggered muxed-D scan cell



Edge-triggered muxed-D scan cell operation

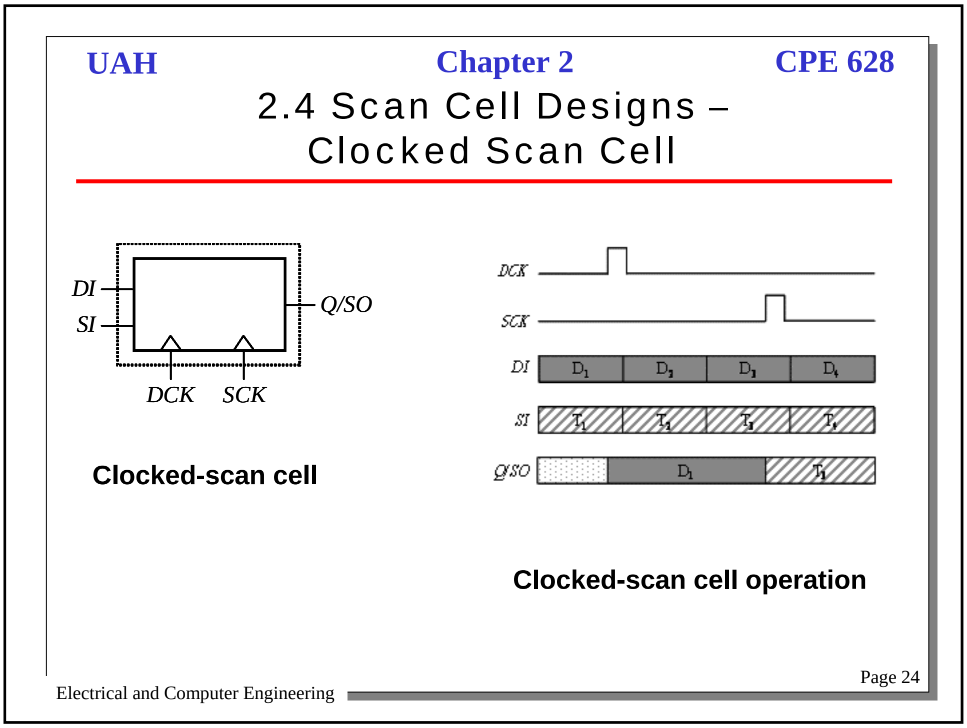


2.4 Scan Cell Designs – Muxed-D Scan Cell(Latch)

Level-sensitive/edge-triggered muxed-D scan cell design

This scan cell is composed of a multiplexer, a D latch, and a D flip-flop.

In this case, _____ operation is conducted in an ___________ manner, while _______ operation and _________ operation is conducted in a ______________ manner.

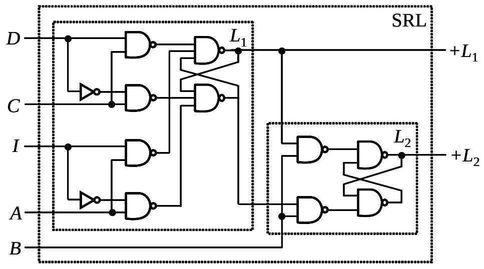


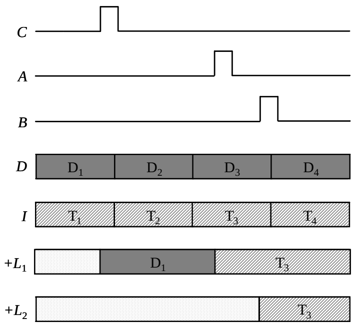
2.4 Scan Cell Designs – Clocked Scan Cell

Clocked-scan cell

Clocked-scan cell operation

2.4 Scan Cell Designs – LSSD Scan Cell



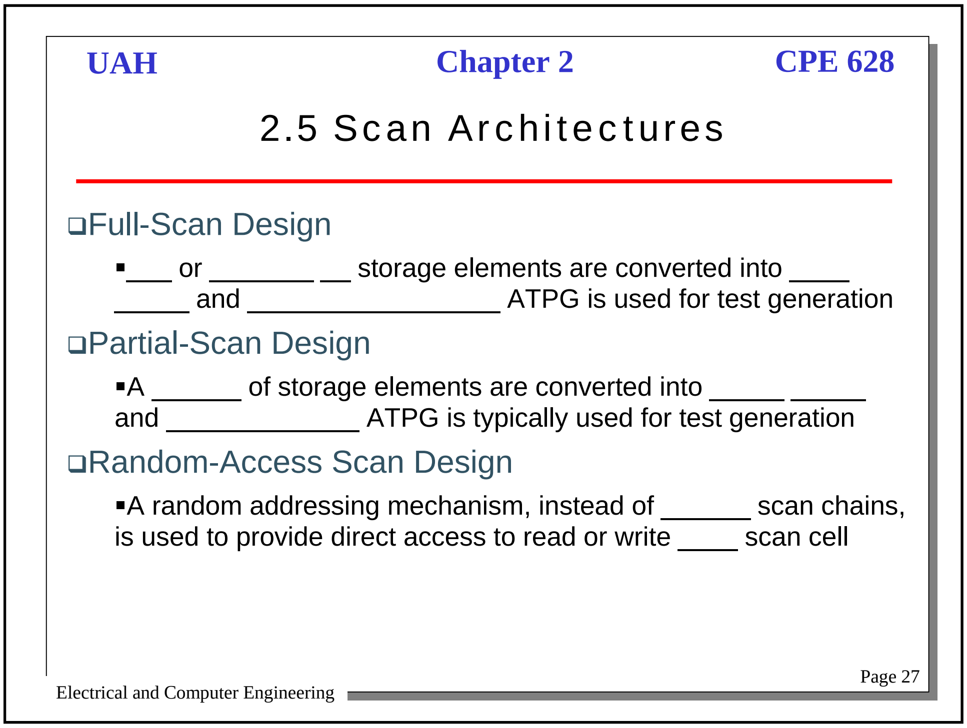


- **Modes of Operation**
  - **Normal**
    - **Fed by __, __ clocks _____**
    - **Fed by __, __ clocks _____ to __, __ clocks data to __**

  Shift
    - **__ clocks ______ _______ to ___, __ clocks _____ to __**

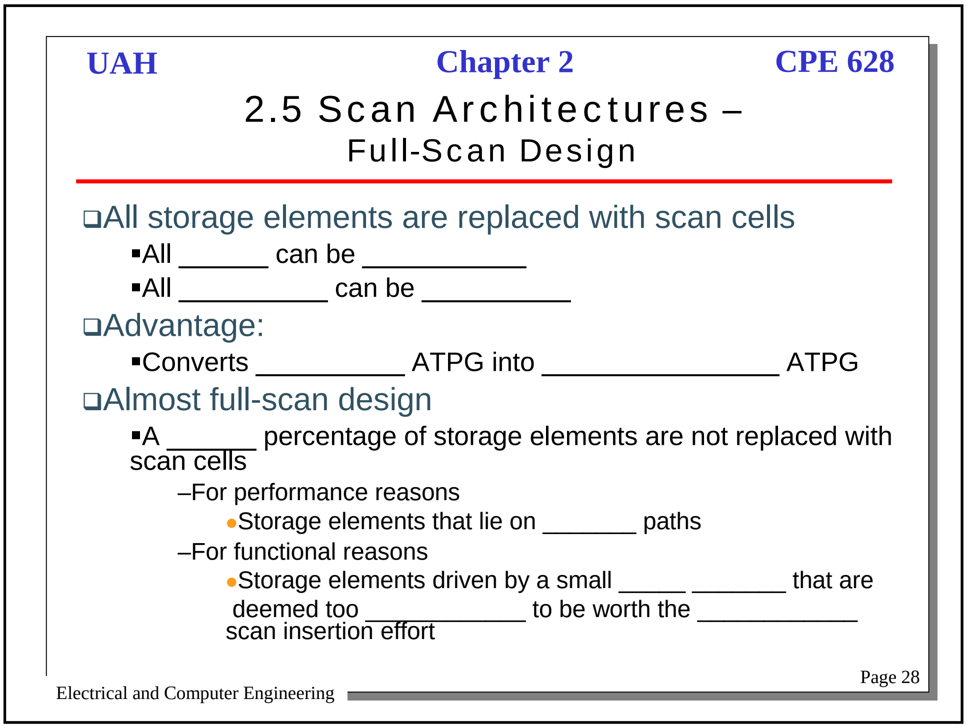
2.4 Scan Cell Designs – Comparison

	Advantages	Disadvantages
Muxed-D Scan Cell	_____________ to modern designs ______________ _______ provided by _________ design automation tools	Add a multiplexer _____
Clocked-Scan Cell	No ______________ degradation	Require additional _____ _____ routing
LSSD Scan Cell	Insert scan into a ___________ design Guaranteed to be _________	Increase ________ complexity



2.5 Scan Architectures

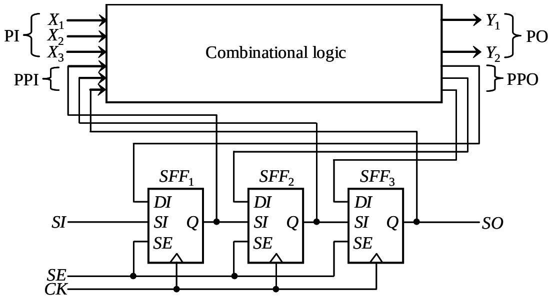
- Full-Scan Design
  - ___ or _______ __ storage elements are converted into ____ _____ and _________________ ATPG is used for test generation
- Partial-Scan Design
  - A ______ of storage elements are converted into _____ _____ and _____________ ATPG is typically used for test generation
- Random-Access Scan Design
  - A random addressing mechanism, instead of ______ scan chains, is used to provide direct access to read or write ____ scan cell



2.5 Scan Architectures –
Full-Scan Design

- All storage elements are replaced with scan cells
  - All ______ can be ___________
  - All __________ can be __________
- Advantage:
  - Converts __________ ATPG into ________________ ATPG
- Almost full-scan design
  - A ______ percentage of storage elements are not replaced with scan cells
    - For performance reasons
      - Storage elements that lie on _______ paths
    - For functional reasons
      - Storage elements driven by a small _____ _______ that are deemed too ___________ to be worth the ___________ scan insertion effort

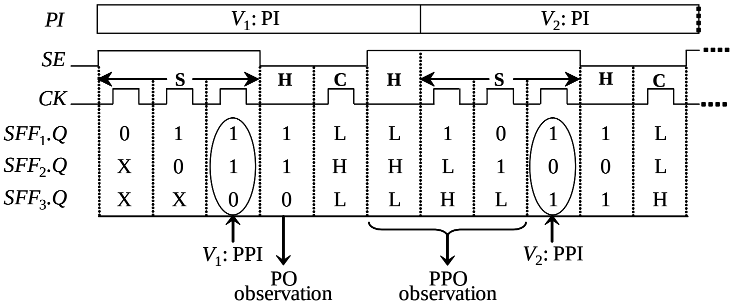
2.5 Scan Architectures –
Full-Scan Design(Muxed-D)



- *Primary inputs* (PIs)
  - –_________ inputs
  - –can be set to ____ _______ logic values
  - –set directly in _______
- *Pseudo primary inputs* (PPIs)
  - –the scan cell ________
  - –can be set to ___ _________ logic values
  - –are set _______ through scan chain ______
- *Primary outputs* (POs)
  - –________ outputs
  - –can be ________
  - –are observed directly in _________

- *Pseudo primary outputs* (PPOs)
  - the scan cell _______
  - can be __________
  - are observed _________ through ____ _____ outputs

2.5 Scan Architectures –
Full-Scan Design(Muxed-D)

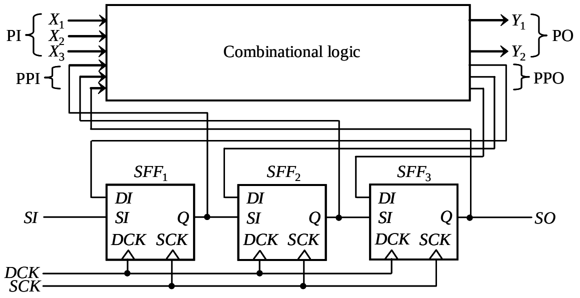


	S	S	S	H	C	H	S	S	S	H	C
$SFF_1.Q$	0	1	1	1	L	L	1	0	1	1	L
$SFF_2.Q$	X	0	1	1	H	H	L	1	0	0	L
$SFF_3.Q$	X	X	0	0	L	L	H	L	1	1	H

S: shift operation / **C**: capture operation / **H**: hold cycle

Test Operations

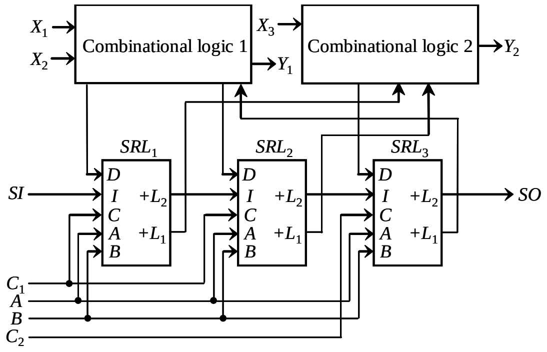
2.5 Scan Architectures –
Full-Scan Design(Clocked)



In a muxed-D full-scan circuit, a scan enable signal *SE* is used.

In a clocked full-scan design, two operations are distinguished by properly applying the two independent clocks *SCK* and *DCK* during shift mode and capture mode.

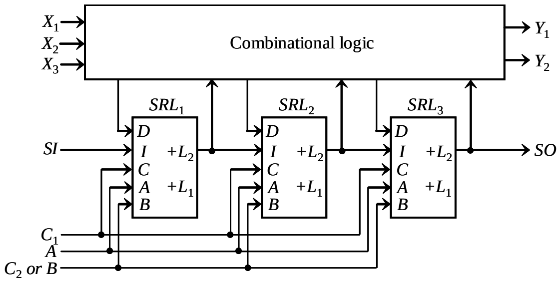
2.5 Scan Architectures –
Full-Scan Design(LSSD)



Single Latch Design

- The output port $+L_1$ of the ______ latch L_1 is used to drive the combinational logic of the design.
- In this case, the ______ latch L_2 is only used for scan testing.
- To prevent combinational feedback, ___ is fed by only __, ___ is fed by only __.

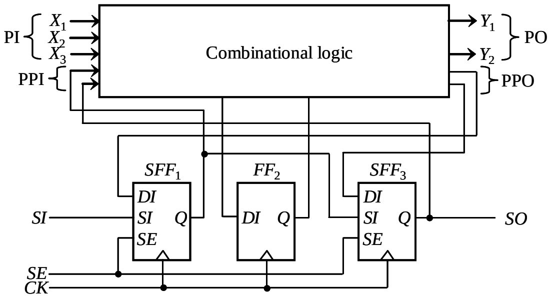
2.5 Scan Architectures –
Full-Scan Design(LSSD)



- In _______ mode, use ___ and ___
- During the _____ operation, use __ and __.
- During the _____ operation, use __ and ___

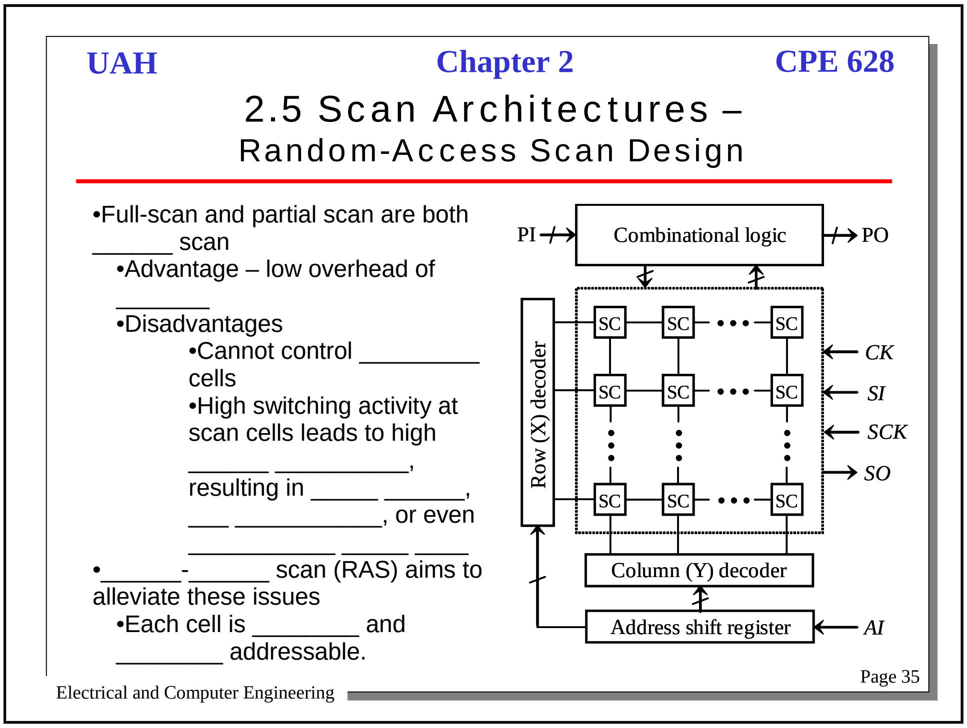
Double Latch Design

2.5 Scan Architectures –
Partial-Scan Design



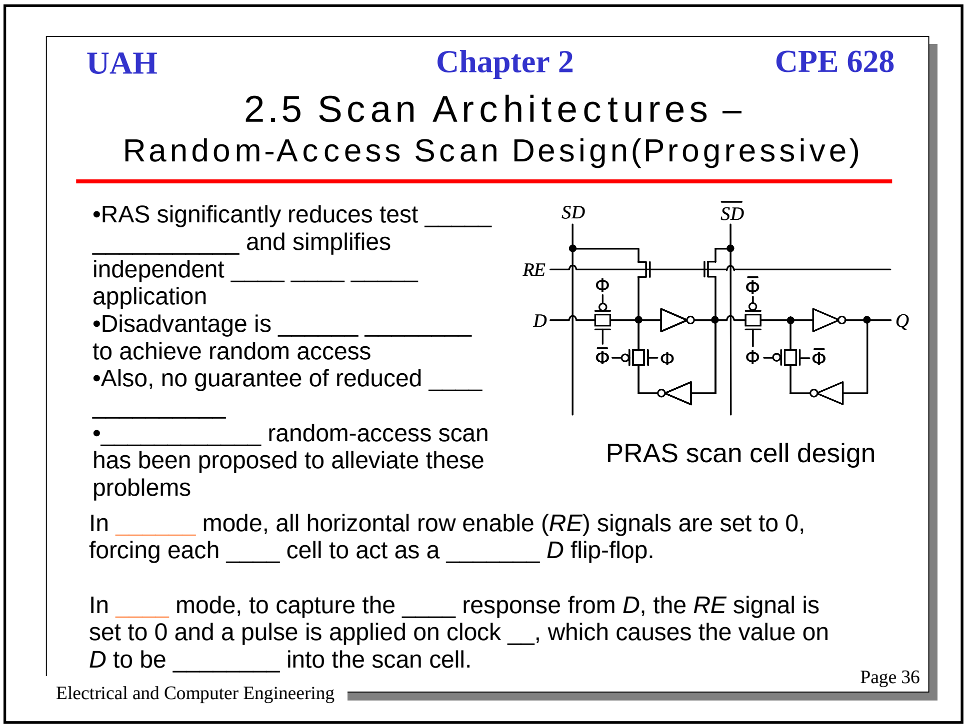
- Advantages
  - Reduces ____ and ________ ____________ ______________
- Disadvantages
  - Results in _____ _____ ________ and _______ _____ generation ____
  - Offers less support for _____, ________ ________ compared to full-scan

Partial-Scan Design



2.5 Scan Architectures –
Random-Access Scan Design

- •Full-scan and partial scan are both _______ scan
  - •Advantage – low overhead of ________
  - •Disadvantages
    - •Cannot control __________ cells
    - •High switching activity at scan cells leads to high _______ ___________, resulting in ______ _______, ____ _____________, or even ____________ ______ _____
- •_______-_______ scan (RAS) aims to alleviate these issues
  - •Each cell is _________ and _________ addressable.



2.5 Scan Architectures –
Random-Access Scan Design(Progressive)

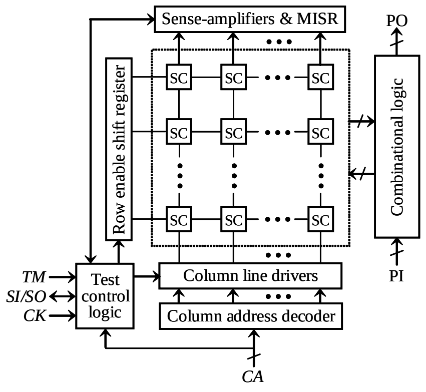
- •RAS significantly reduces test _____ ____________ and simplifies independent ____ ____ _____ application
- •Disadvantage is _______ _________ to achieve random access
- •Also, no guarantee of reduced ____ ___________
- •_____________ random-access scan has been proposed to alleviate these problems

PRAS scan cell design

In _______ mode, all horizontal row enable (*RE*) signals are set to 0, forcing each _____ cell to act as a ________ *D* flip-flop.

In _____ mode, to capture the _____ response from *D*, the *RE* signal is set to 0 and a pulse is applied on clock __, which causes the value on *D* to be _________ into the scan cell.

2.5 Scan Architectures –
Random-Access Scan Design(Progressive)



PRAS Architecture

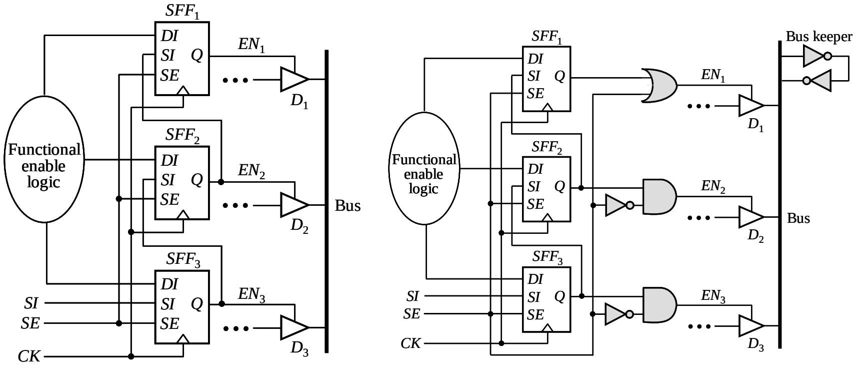
```
for each test vector $v_i$ ($i$ = 1, 2, …, $N$) {
  /* Test stimulus application */
  /* Test response compression */
  enable TM;
  for each row $r_j$ ($j$ = 1, 2, …, $m$) {
    read all scan cells in $r_j$ / update MISR;
    for each scan cell SC in $r_j$
      /* $v$(SC): current value of SC */
      /* $v_i$(SC): value of SC in $v_i$ */
        if $v$(SC) $\neq$ $v_i$(SC)
          update SC;
  }
  /* Test response acquisition */
  disable TM;
  apply the normal clock;
}
scan-out MISR as the final test response;
```

2.6 Scan Design Rules

- Problematic _______ _______
  - _____ ______ ____
    - ______ _____
    - ____________ I/O Ports
    - _____ Clocks
  - _____
    - ______ Clocks
    - _______________ Feedback Loops
    - _______________ Set/Reset Signals

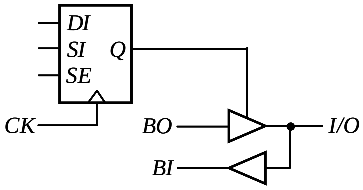
2.6 Scan Design Rules – Tristate Buses

- Problem with ___ __________ may occur during _______
- Fault _________ ____ without __________, or ___ _____



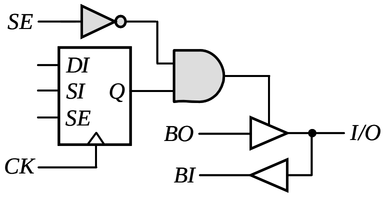
2.6 Scan Design Rules – Bidirectional I/O Ports

- Problem may occur during shifting



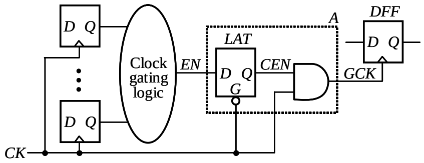
Original Circuit

Pin is input but shifted value may enable BO



Modified Circuit

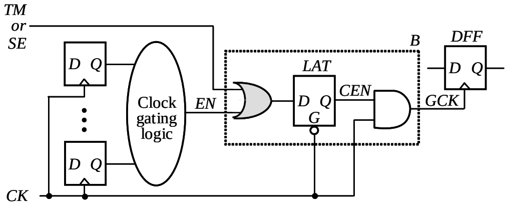
2.6 Scan Design Rules – Gated Clocks



Original Circuit

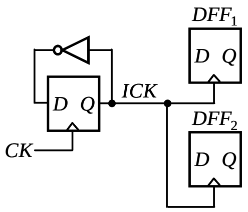
- Clock gating reduces _____ consumption but also means that the clock cannot be __________ from ____ ______ ______

- If ___ is used, ______ only during _____
- If ___ is used, fault coverage on the _____ ______ _____ is lost



Modified Circuit

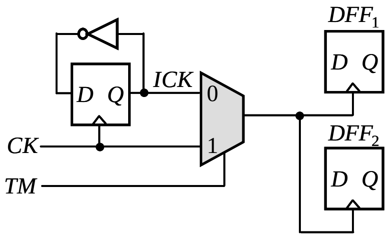
2.6 Scan Design Rules – Derived Clocks



Original Circuit

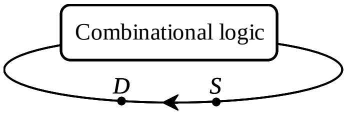
- A derived clock is a clock signal _________ _________ and is not controllable from the ________ _____.

- A derived clock must be _________ during the _____ _____ operation



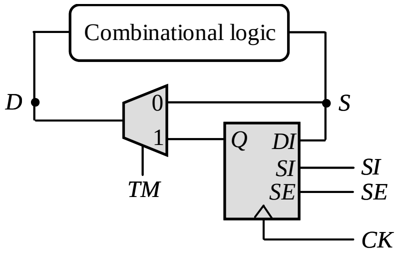
Modified Circuit

2.6 Scan Design Rules – Combinational Feedback Loops



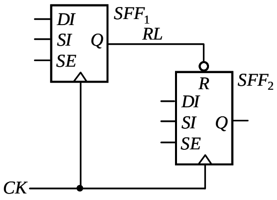
Original Circuit

- Get rid of it if at all possible



Modified Circuit

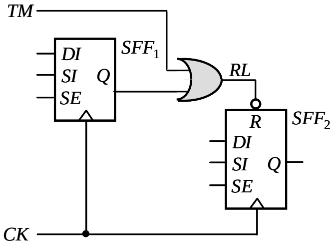
2.6 Scan Design Rules – Asynchronous Set/Reset Signals



Original Circuit

- Asynchronous set/reset signals not ________ ___________ from the primary inputs can prevent ____ ______ from working properly.

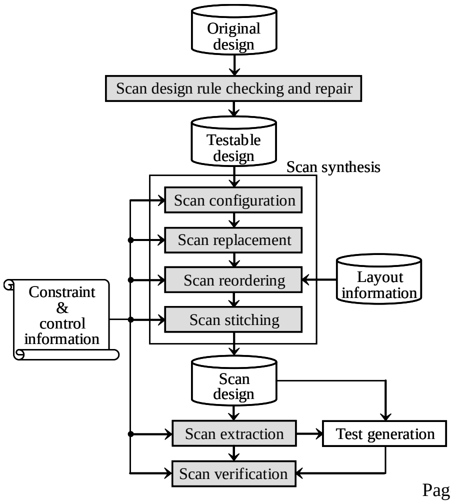
- Using ___ means that faults in the _____________ _________ logic cannot be _______
- Using __ may lead to _____ _________
- Use ___, ______ ________



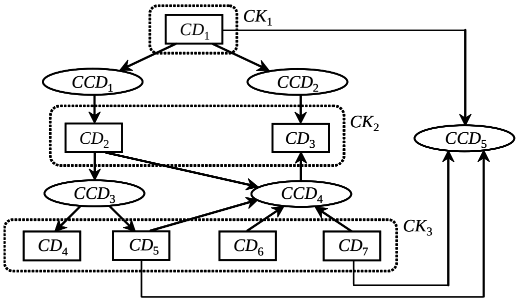
Modified Circuit

2.6 Scan Design Flow

- ❑Scan Design Rule Checking and Repair
  - ▪________ and _______ all scan design rule __________
- ❑Scan Synthesis
  - ▪Converts a ________ design into a ______ design without ________ original functionality
- ❑Scan Extraction
  - ▪________ all scan cell instances from all _____ specified _______
- ❑Scan Verification
  - ▪Verify ____ ____ operation and _____ ________ operation using timing file in *standard delay format* (SDF)



2.6 Scan Design Flow – Scan Design Rule Checking and Repair



During the _________ phase, following design rules should guarantee correctness for data paths that _________ and __________ within the same _____ _______. Moving across ________ is tricky, but can ______ some _______.

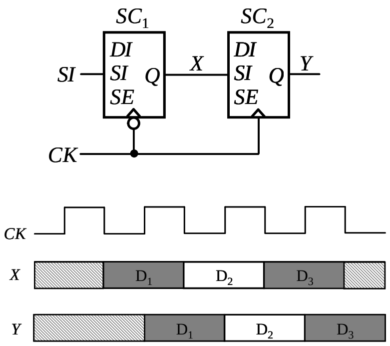
The clock _____ between ________ scan cells must be properly __________ in order not to cause any _____ _______

2.7 Scan Design Flow – Scan Synthesis

- Includes four separate and distinct steps:
  - Scan Configuration
    - The number of ____ _____ used
    - The _____ of scan cells used to ____________ these scan chains
    - Which storage elements to ________ from the process
    - How the scan cells are __________
  - Scan Replacement
    - Replaces all _________ storage elements in the testable design with their _____________________ scan cells
  - Scan Reordering
    - The process of reordering the scan chains based on the ________ scan cell ________, in order to minimize the amount of ___________ _____ used to implement the scan chains
  - Scan Stitching
    - Stitch all ____ _____ together to form ____ ______

2.7 Scan Design Flow – Scan Synthesis(Scan Configuration)

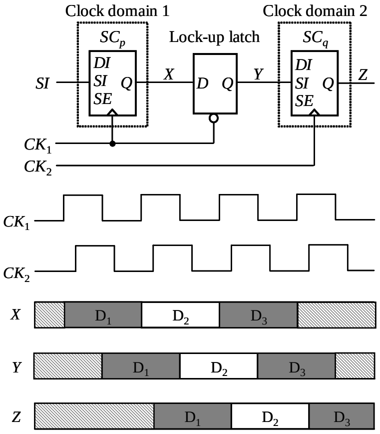
- Scan Configuration
  - The number of scan chains used –limited by ____ _________, share with __________ pins, can't put any on ____ _______ I/O pads, also limited by ________ on tester
  - The types of scan cells used to implement these scan chains – picked from ________ ________
  - Which storage elements to exclude from the process – _______ _______ or _________ reasons
  - How the scan cells are arranged – consider ______ _________ and _________ of scan cells



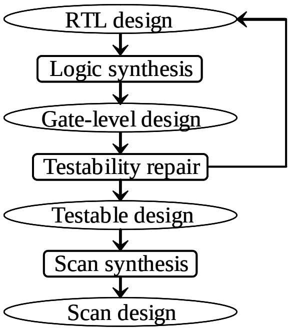
Mixing Falling and Rising Edges

2.7 Scan Design Flow – Scan Synthesis(Scan Configuration)

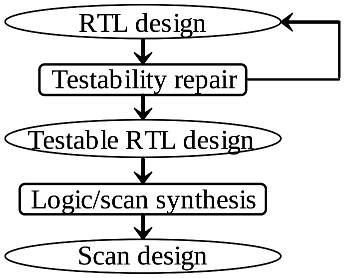
- •Crossing Clock Domains
  - •Lock up latch, or __________, put in to guarantee that any _____ _____ between the clocks can be _________
  - •Clock skew is not ________ across _____ _______
  - •This scheme works only when the _______ _____ between the clocks is less than the _____ of the clock pulse



2.9 RTL Design for Testability



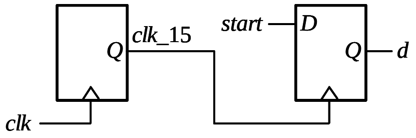
Gate-Level Testability Repair Design Flow



RTL-Level Testability Repair Design Flow

2.9 RTL Design for Testability – RTL Scan Design and Repair(Example)

```
always @(posedge clk)
   if (q == 4'b1111)
      clk_15 <= 1;
   else
      begin
         clk_15 <= 0;
         q <= q + 1;
      end
always @(posedge clk_15)
   d < = start;
```

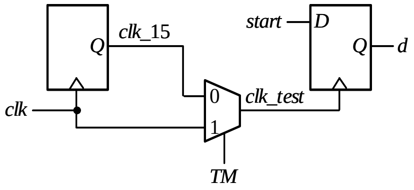


RTL Verilog Description

Generated Schematic

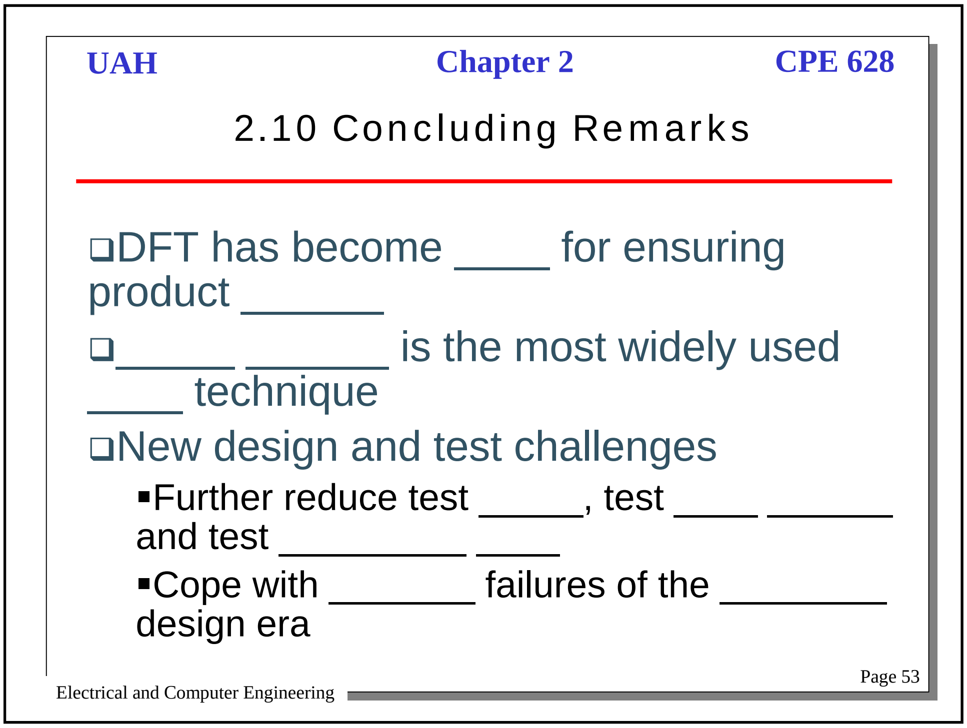
2.9 RTL Design for Testability – RTL Scan Design and Repair(Example)

```
always @(posedge clk)
   if (q == 4'b1111)
      clk_15 <= 1;
   else
      begin
         clk_15 <= 0;
         q <= q + 1;
      end
assign clk_test = (TM)? clk : clk_15;
always @(posedge clk_test)
   d < = start;
```



Repaired RTL Verilog Description

Repaired Schematic



2.10 Concluding Remarks

- ❑DFT has become _____ for ensuring product _______
- ❑______ _______ is the most widely used _____ technique
- ❑New design and test challenges
  - ▪Further reduce test _____, test ____ ______ and test _________ ____
  - ▪Cope with _______ failures of the ________ design era