CPE 628
Chapter 1 - Introduction

Dr. Rhonda Kay Gaede

UAH

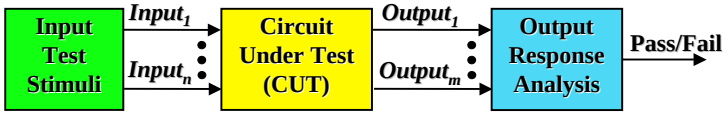
Electrical and Computer Engineering

1.1 Importance of Testing

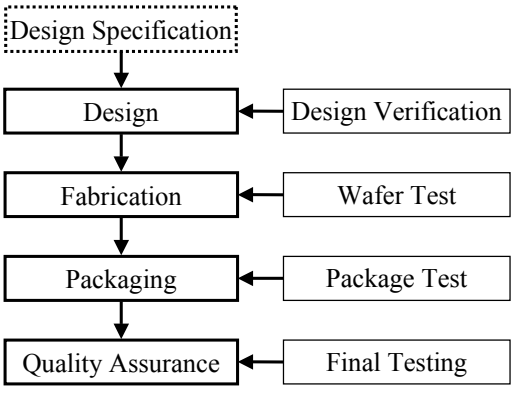
- Every component(instance of a design) has to work so it must be tested before being used.
- If we don't test at every level, we've wasted resources.
- When components were small, exhaustive testing was easy.
- Components are no longer small, but feature sizes are.
- With small feature sizes, defects can turn more easily into failures.
- Testing is also done while a component is operational.

1.2 Testing During the VLSI Lifecycle

- Basic testing approach

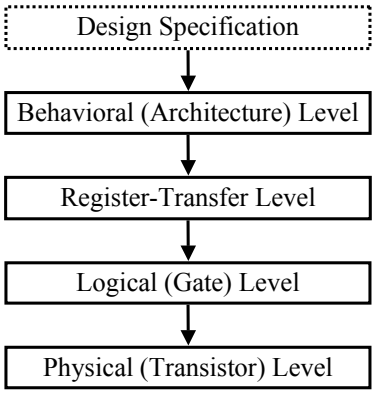


1.2 Testing During the VLSI Lifecycle – VLSI Development Process



- A defect is a flaw or physical imperfection that may lead to a fault.
- Failure mode analysis is typically used at all stages of IC manufacturing testing to identify improvements to processes.

1.2 Testing During the VLSI Lifecycle – VLSI Development Process (Verification)



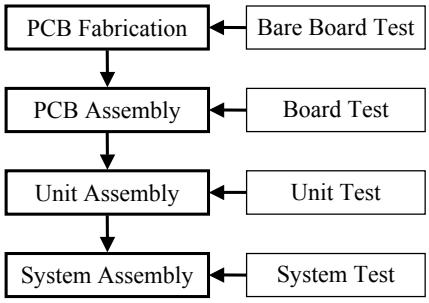
- Design verification is economically significant because it has an impact on time-to-market
- Design verification stimuli are often used to test during the manufacturing process.

1.2 Testing During the VLSI Lifecycle – VLSI Development Process (Yield, Reject Rate)

- The yield of a manufacturing process is defined as the percentage of acceptable parts among all parts that are fabricated.
  - Yield =
- Two types of yield loss
  - Catastrophic – due to random defects
  - Parametric – due to process variations
- Two types of errors in testing
  - False positive – faulty device appears to be good
  - False negative – good device appears to be bad
- The ratio of field-rejected parts to all parts passing quality assurance testing is referred to as the reject rate.
  - Reject rate =
  - 500 PPM acceptable, 100 PPM high quality, 3.4 PPM six sigma

1.2 Testing During the VLSI Lifecycle – Electronic System Manufacturing Process

- Higher level systems are assembled from VLSI devices
- These manufacturing steps are also susceptible to defects
- PCB manufacturing is somewhat similar to IC manufacturing as both are photolithographic processes



- Unit and system level testing typically don't use the same tests as those used for PCBs and VLSI devices.

1.2 Testing During the VLSI Lifecycle – Electronic System Manufacturing Process

- During system operation, a number of events can result in a system failure
  - Single-bit upsets, Electromigration, Material aging
- The operational and repair times are assumed to be exponentially distributed random numbers.
- The probability that a system will operate normally until time t, reliability, is $P(T_n > t) = e^{-\lambda t}$, where λ is the failure rate.
- The repair time, R, is similarly $P(R > t) = e^{-\mu t}$, where μ is the repair rate.
- MTBF = MTTR =
- Availability =

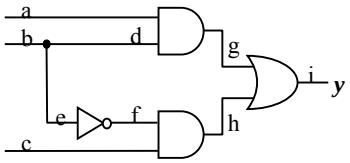
1.3 Challenges in VLSI Testing – Test Generation

- Structural Testing - alternative to exhaustive
  - Need a fault model – a set of things that can go wrong
  - Fault coverage =
  - Some faults are undetectable
  - Effective fault coverage =
  - Defect level =
  - A test vector is a set of inputs that will produce a faulty output if a fault occurs.
  - Test generation is the process of finding an efficient set of test vectors that detect all faults modeled in the process.
  - Test vectors are also used in the fault simulation process.

1.3 Challenges in VLSI Testing – Fault Models

- A good fault model should
  - Accurately reflect the behavior of defects
  - Be computationally efficient
- Unfortunately, no single fault model accurately reflects the behavior of all defects
- Multiple fault models are used
- Single fault assumption
  - Number of single faults = k x n, where k is the number of different types of faults and k is the number of locations considered
- Multiple fault reality
  - Number of multiple faults = $(k + 1)^n - 1$
- Two faults may be equivalent, fault collapsing involves reducing the set of faults by removing equivalent faults.

1.3 Challenges in VLSI Testing – Fault Models(Stuck-At Faults)



Faults are inserted at primary inputs, primary outputs, internal gate inputs and outputs, including fanout gates

$x_1x_2x_3$	000	001	010	011	100	101	110	111
y	0	1	0	0	0	1	1	1
a SA0	0	1	0	0	0	1	0	0
a SA1	0	1	1	1	0	1	1	1
b SA0	0	1	0	1	0	1	0	1
b SA1	0	0	0	0	1	1	1	1
c SA0	0	0	0	0	0	0	1	1
c SA1	1	1	0	0	1	1	1	1
d SA0	0	1	0	0	0	1	0	0
d SA1	0	1	0	0	1	1	1	1
e SA0	0	1	0	1	0	1	1	1

$x_1x_2x_3$	000	001	010	011	100	101	110	111
y	0	1	0	0	0	1	1	1
e SA1	0	0	0	0	0	0	1	1
f SA0	0	0	0	0	0	0	1	1
f SA1	0	1	0	1	0	1	1	1
g SA0	0	1	0	0	0	1	0	0
g SA1	1	1	1	1	1	1	1	1
h SA0	0	0	0	0	0	0	1	1
h SA1	1	1	1	1	1	1	1	1
i SA0	0	0	0	0	0	0	0	0
i SA1	1	1	1	1	1	1	1	1

1.3 Challenges in VLSI Testing – Fault Models(More Stuck-At Faults)

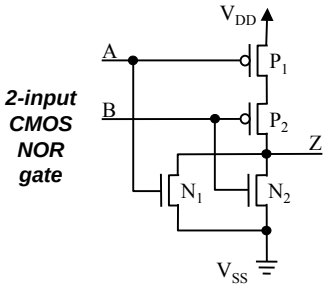
$x_1x_2x_3$	000	001	010	011	100	101	110	111
y	0	1	0	0	0	1	1	1
a SA0	0	1	0	0	0	1	0	0
a SA1	0	1	1	1	0	1	1	1
b SA0	0	1	0	1	0	1	0	1
b SA1	0	0	0	0	1	1	1	1
c SA0	0	0	0	0	0	0	1	1
c SA1	1	1	0	0	1	1	1	1
d SA0	0	1	0	0	0	1	0	0
d SA1	0	1	0	0	1	1	1	1
e SA0	0	1	0	1	0	1	1	1

$x_1x_2x_3$	000	001	010	011	100	101	110	111
y	0	1	0	0	0	1	1	1
e SA1	0	0	0	0	0	0	1	1
f SA0	0	0	0	0	0	0	1	1
f SA1	0	1	0	1	0	1	1	1
g SA0	0	1	0	0	0	1	0	0
g SA1	1	1	1	1	1	1	1	1
h SA0	0	0	0	0	0	0	1	1
h SA1	1	1	1	1	1	1	1	1
i SA0	0	0	0	0	0	0	0	0
i SA1	1	1	1	1	1	1	1	1

Collapsing faults typically reduces the number of faults by ___ to ___ %.

1.3 Challenges in VLSI Testing – Fault Models(Transistor Faults)

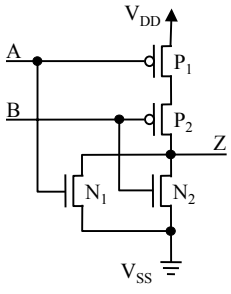
- **At the switch level, a transistor can be _____ or _____, this behavior cannot be reflected in the _____ model.**
- **Consider a two-input CMOS NOR gate.**
- **Suppose transistor N_2 is _____. When the input vector AB = ___ is applied, output Z should be a logic __, but the stuck-open fault causes Z to be _____ _____ _____ and Z keeps ___ _____ _____. Need AB = __ → __**
- **What if N_2 is _____? There is a _____ ____ from V_{DD} to V_{SS} when AB = __, it's a _____ _____, catch this with ____ testing.**



2-input CMOS NOR gate

- Transistor faults can also be _____. Serial _____ faults are equivalent and parallel _____ faults are equivalent.

1.3 Challenges in VLSI Testing – Fault Models(Transistor Faults)



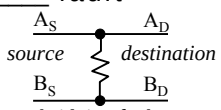
2-input CMOS NOR gate

Truth table for fault-free circuit and all possible transistor faults

AB	00	01	10	11
Z	1	0	0	0
N_1 stuck-open	1	0	last Z	0
N_1 stuck-short	I_{DDQ}	0	0	0
N_2 stuck-open	1	last Z	0	0
N_2 stuck-short	I_{DDQ}	0	0	0
P_1 stuck-open	last Z	0	0	0
P_1 stuck-short	1	0	I_{DDQ}	0
P_2 stuck-open	last Z	0	0	0
P_2 stuck-short	1	I_{DDQ}	0	0

1.3 Challenges in VLSI Testing – Fault Models(Open and Short Faults)

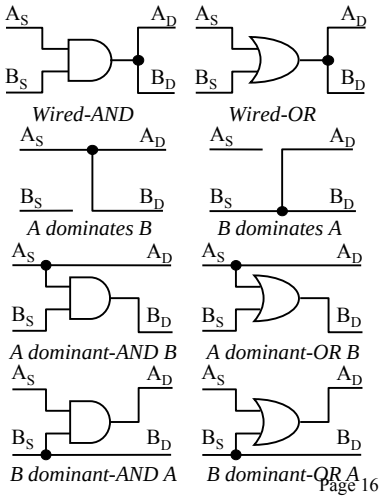
- Defects in VLSI devices can include _____ and _____ in the _____.
- _____
  - On wires that form _____ behave like _____ faults
  - On wires that _____ _____ behave like _____ faults
  - A _____ _____ acts like a _____ _____
- _____
  - Commonly referred to as a _____ fault
  - To _____ or _____ acts like _____ fault
  - _____ _____ multiple models



1.3 Challenges in VLSI Testing – Fault Models(Bridging Faults)

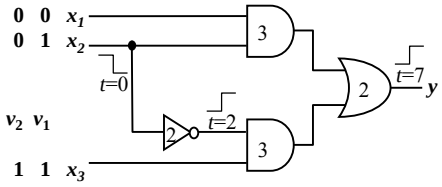
- Three models
  - _____
  - _____
  - _____

A_S B_S	0 0	0 1	1 0	1 1
A_D B_D	0 0	0 1	1 0	1 1
Wired-AND	0 0	0 0	0 0	1 1
Wired-OR	0 0	1 1	1 1	1 1
A dominates B	0 0	0 0	1 1	1 1
B dominates A	0 0	1 1	0 0	1 1
A dominant-AND B	0 0	0 0	1 0	1 1
B dominant-AND A	0 0	0 1	0 0	1 1
A dominant-OR B	0 0	0 1	1 1	1 1
B dominant-OR A	0 0	1 1	1 0	1 1



1.3 Challenges in VLSI Testing – Fault Models(Delay Faults and Crosstalk)

- A _____ _____ causes excessive _____ along a path such that the total _____ _____ falls _____ the specified limit
- Delay Fault Models
  - _____, _____ – gate output transition
  - _____ – _____ propagation delay along a _____
  - Delay faults require an _____ _____ of test vectors



- Only gate delay is shown here but the reality is that _____ _____ is now about ___ % __ _____ of the total delay

- Crosstalk effects
  - Glitches – a _____ provoked by coupling effects
  - Delays – _____ _____ caused by coupling effects
  - Active area of research

1.3 Challenges in VLSI Testing – Fault Models(Pattern Sensitivity and Coupling Faults)

- _____ circuits have special _____ – example _____
- The _____ of a cell or the _____ of a memory cell to _____ can be influenced by the contents of its _____ cells (_____ _____)
- A _____ fault occurs when a _____ in one cell causes the _____ of another cell to change
- Many memory test _____ have been proposed, most involve _____ _____ and _____ and _____ patterns

Notation:
w0 = write 0 (or all 0's)
r1 = read 1 (or all 1's)
↑ = address up
↓ = address down
↕ = address either way

Test Algorithm	March Test Sequence
March LR w/o BDS	↕(w0); ↓ (r0, w1); ↑ (r1, w0, r0, r0, w1); ↑ (r1, w0); ↑ (r0, w1, r1, r1, w0); ↑ (r0)
March LR with BDS	↕(w00); ↓ (r00, w11); ↑ (r11, w00, r00, r00, w11); ↑ (r11, w00); ↑ (r00, w11, r11, r11, w00); ↑ (r00, w01, w10, r10); ↑ (r10, w01, r01); ↑ (r01)

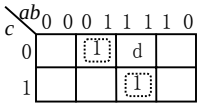
1.3 Challenges in VLSI Testing – Fault Models(Analog Fault Models)

- **Analog circuits are constructed with _____ and _____ components**
- **_____ faults – _____, _____**
- **_____ faults – components are out of _____ ranges**
- **_____ circuits can have faults that affect AC and/or DC characteristics**
- **Analog fault models are _____ to come by**

1.4 Levels of Abstraction in VLSI Testing – Register-Transfer Level and Behavioral Level

- **Design done at _____ and _____ level**
- **Fault models are from _____ and _____ levels**
- **Test generation works at the ____ level**
- **Example – Influence of Structure**

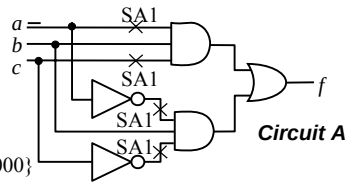
$f(a,b,c)=\Sigma_m(1,7)+d(3) = \bar{a}\bar{b}\bar{c} + abc$



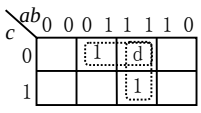
Circuit A

$f = abc + \bar{a}\bar{b}\bar{c}$

Test Vectors
{111,110,101,011,010,000}



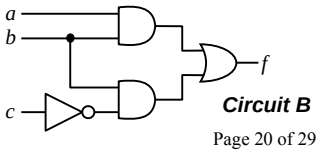
Circuit A



Circuit B

$f = ab + b\bar{c}$

Test Vectors
{111,101,010,000}



Circuit B

1.4 Levels of Abstraction in VLSI Testing – Gate, Switch, and Physical

- _____ level - has been used for _____, however it is now widely believed that _____ _____ at the _____ level is not sufficient for _____ design.
- _____ Level - For _____ _____ implementation, transistor fault models can be applied and evaluated based on the gate-level _____. When _____ models are substituted, we obtain an accurate _____ of the netlist used for _____ _____. In addition, _____ _____ and _____ _____ faults can also be tested at the _____ _____.
- _____ Level – The _____ _____ level for VLSI testing because it provides the _____ _____ and _____ information. It is used to characterize _____ properties such as _____, _____ and _____.

1.5 Historical Review of VLSI Test Technology

- **Two Processes**
  - **Test _____**
  - **Test _____**
    - _____ _____ _____
    - **Test Facilities** __ _____ _____

1.5 Historical Review of VLSI Test – Automatic Test Equipment

- Generally, ATE consists of the following parts
  - _____
  - ___ _____ and Fixtures
    - Data Generator – _____ _____
    - Pin Electronics – _____ vectors to produce _____, also _____ outputs
  - Test Program – usual stuff plus ____ ___ (_____, ____, _____ type - RZ, NRZ etc.)
  - Digital Signal Processor
  - Accurate DC and AC Measurement Circuitry
- Cost Containment Measures
  - _____
  - _____
  - _____ Test Capabilities
  - _____ Components

1.5 Historical Review of VLSI Test – Automatic Test Pattern Generation

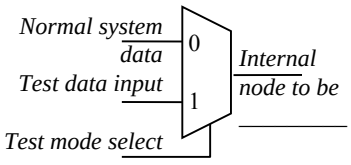
- A complete ATPG algorithm, the _____, was first published in _____. The complexity grew as the number of ____ _____.
- The next landmark effort in ATPG was _____ which reduced the complexity to that of the number of _____ _____.
- ____ and _____ were further improvements.
- Over time, it was realized that a lot of faults were _____ to test so instead of starting with the _____ _____ of faults for ATPG, an initial phase used _____ _____ followed by _____ _____ to reduce the number of faults for which ATPG was necessary.
- Combinational and sequential benchmarks were introduced in 1984 and 1989 respectively.
- The combinational problem ___ _____ _____ and the sequential problem is _____ if design for test (DFT) techniques are used.

1.5 Historical Review of VLSI Test – Fault Simulation and Design for Testability

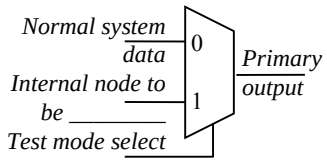
- **Improved Approaches**
  - _____ **Fault Simulation**
  - _____ **Fault Simulation**
  - _____ **Fault Simulation**
- **Design for Testability is the _____ of design and test, it's been around since the 1970s**
  - __ _____ **DFT techniques**
  - _____ _____
  - _____ _____

1.5 Historical Review of VLSI Test – Design for Testability Techniques

- **Ad hoc DFT Techniques**
  - Add _____ test _____ (usually _____) for
    - _____
    - _____
  - Added on a _____ basis
    - Primarily targets _____ portions of chip



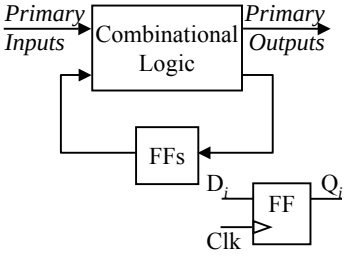
_____ test point

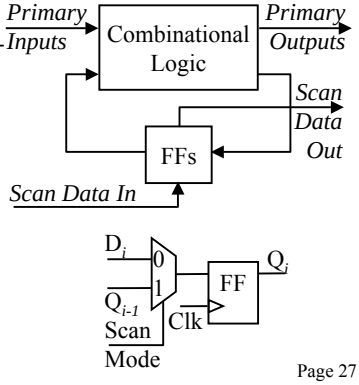


_____ test point

1.5 Historical Review of VLSI Test – Design for Testability Techniques

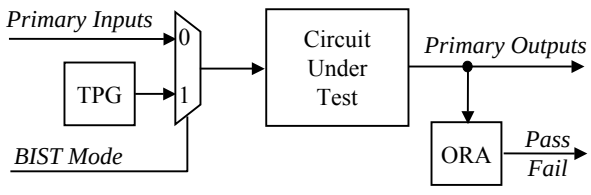
- Scan Techniques
  - Transforms _____ of chip into a _____ _____
  - Scan mode facilitates
    - Shifting __ _____ _____
    - Shifting ___ _____





1.5 Historical Review of VLSI Test – Design for Testability Techniques

- BIST Technique
  - Integrate _____ _____ and _____ _____ _____ in the VLSI device itself
  - BIST can be used at ___ _____ of testing, from _____ through _____ testing



1.5 Historical Review of VLSI Test – Board and Boundary Scan Testing

- Boundary Scan
  - Developed to get access to _____ on _____ boards
  - Logic is inserted to provide a _____ _____ through all ___ _____ of an IC
  - Enables __ and _____ testing

TAP pin	I/O	Function
TCK	input	Test clock
TMS	input	Test Mode Select
TDI	input	Test Data In
TDO	output	Test Data Out