CPE 426 Spring 2002 Midterm Solutions:

1.

```
use work.LOGIC_PKG.all;

entity EXPRESSION is
  port (A, B, C, D : in BIT;
        F : out BIT);
end EXPRESSION;

architecture STRUCTURAL of EXPRESSION is
  signal ABAR, BBAR, CBAR, G, H, I : BIT;
begin
  U1 : NAND2_OP port map(A, A, ABAR);
  U2 : NAND2_OP port map(B, B, BBAR);
  U3 : NAND2_OP port map(C, C, CBAR);
  U4 : AND3_OP port map(ABAR, BBAR, D, G);
  U5 : AND3_OP port map(A, B, C, H);
  U6 : AND3_OP port map(BBAR, CBAR, '1', I);
  U7 : OR4_OP port map(G, H, I, '0', F);
end STRUCTURAL;
```

2. A port is a signal used in describing the interface of a VHDL model.

3.

```
package dumb is
  function count_ones (x : in BIT_VECTOR) return integer;
end dumb;

package body dumb is
  function count_ones (x : in BIT_VECTOR) return integer is
    variable count : integer;
  begin
    count := 0;
    for  i in x'range loop
      if (x(i) = '1') then
        count := count + 1;
      end if;
    end loop;
    return count;
  end count_ones;
end dumb;

use work.dumb.all;

entity test is
end test;

architecture ones_count of test is
  signal test1 : bit_vector(7 downto 0) := "01010111";
  signal test2 : bit_vector(7 downto 0) := "00000000";
begin
  process
    variable count : integer;
  begin
```

```
    count := count_ones(test1);
    count := count_ones(test2);
    wait;
  end process;
end ones_count;
```

4. For the following function call, which function will be called?
__A___
```
VARIABLE a, b : INTEGER;
b := decrement (a);
(a) FUNCTION decrement (x : INTEGER) RETURN INTEGER;
(b) FUNCTION decrement (x : REAL) RETURN REAL;
```

5. 'event is an example of a VHDL attribute.

6.
```
entity LED_DRIVER is
  port (D : in BIT_VECTOR (1 downto 0);
        S : out BIT_VECTOR(6 downto 0));
end LED_DRIVER;

architecture CONCURRENT of LED_DRIVER is
begin
  S <= "1111011" when D = "00" else
       "0001010" when D = "01" else
       "0110111" when D = "10" else
       "0011111";
end CONCURRENT;
```

7. Solution not given.

8. An entity X, when used in another entity Y, becomes a component for the entity Y.

9. BIT_VECTOR is an example of an unconstrained array.

10. Transport delay is the delay which represents wire delay in VHDL.

11. All statements inside of a process are sequential.

12.
```
library ieee;
use ieee.std_logic_1164.all;

package TEST_TYPES is
  type MVL4 is ('X', 'Z', '0', '1');
  type DAY_OF_WEEK is (Sunday, Monday, Tuesday, Wednesday,
                       Thursday, Friday, Saturday);
  subtype BUFFER_NUMBER is integer range 0 to 7;
  subtype COST is real range 0.0 to 1405.0;
  subtype DEC_16 is integer range 15 downto 0;
  type REG_16_DESCENDING is array (DEC_16) of MVL4;
  type TABLE_3D is array (std_logic, std_logic, std_logic)
                   of std_logic;
end TEST_TYPES;
```

13.

state	sig_in = '0'	sig_in = '1'
	next_state, sig_out	next_state, sig_out
a	a, '1'	d, '0'
b	b, '0'	c, '1'
c	b, '0'	a, '1'
d	e, '1'	e, '0'
e	e, '0'	c, '0'