The University of Alabama in Huntsville
ECE Department
CPE 526 01
Midterm Exam
February 26, 2002

1. (20 points) Describe the following logic expression

(A'• B' • D) + (A • B • C) + (B' • C')

with a structural VHDL model using the following package located in library WORK.

Hint: If you don't need all of the inputs, you can tie one or more of them to '0' or '1'.

```
package LOGIC_PKG is
  component AND3_OP
    port A, B, C : in BIT; Z out BIT);
  end component;
  component NAND2_OP
    port A, B : in BIT; Z out BIT);
  end component;
  component OR4_OP
    port A, B, C, D : in BIT; Z out BIT);
  end component;
end LOGIC_PKG;
```

2. (1 point) A _____ is a signal used in describing the interface of a VHDL model.

3. (15 points) Write a function that accepts a bit vector of arbitrary length and returns an integer that is the total number of ‘1’s contained in the bit vector.

4. (1 point) _____ delay is the delay which represents wire delay in VHDL.

5. (1 point) All statements inside of a process are _____.

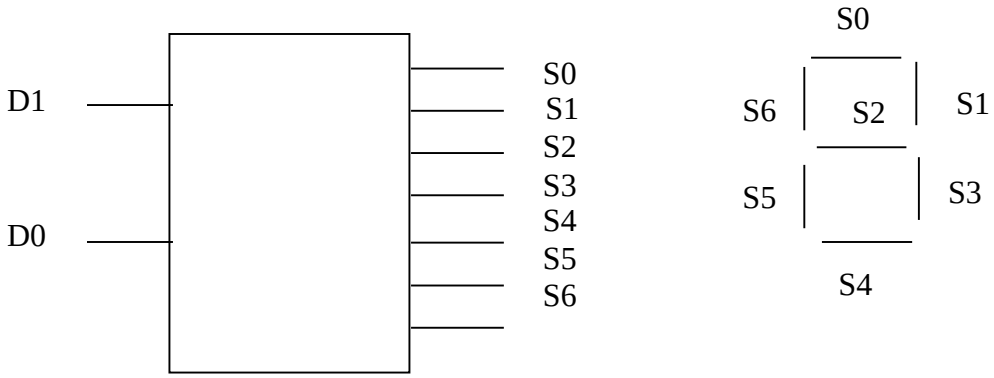
6. (2 points) For the following function call, which function will be called? _____

```
VARIABLE a, b : INTEGER;
b := decrement (a);
```

(a) `FUNCTION decrement (x : INTEGER) RETURN INTEGER;`
(b) `FUNCTION decrement (x : REAL) RETURN REAL;`

7. (1 point) _____ is an example of a VHDL attribute.

8. (12 points) Consider the following combinational digital system, called a light-emitting diode (LED) driver. The LED driver converts a 2-bit binary number (D_1D_0) into an LED-displayed numeral. For example, $D_1D_0 - 10_2$ is displayed by asserting S_0, S_1, S_2, S_4, and S_5.



(a)(3 points) Write an entity for the LED driver. (b)(9 points) Use concurrent signal assignments to model the LED driver.

9. (5 points) Consider the following structural VHDL model.

```
entity SMODEL is
   port
     (P1 : in BIT;
      P2 : out BIT;
      P3 : inout BIT);
end SMODEL;

architecture STRUCTURE of SMODEL is
   component UNIT
      port (C1, C2, : in BIT; C3 : out BIT);
   end component;

begin
  U1 : UNIT port map (C1 => ?, C2 => ?, C3 => ?);
end STRUCTURE;
```

(a) (3 points) Complete the structural description by giving a legal set of port-to-port connections for entity ports P1, P2, and P3 and component ports C1, C2, and C3.

(b) (2 points) Is there more than one possible set of legal port-to-port connections?

10. (10 points) Write a VHDL description for a D-type latch with asynchronous set and reset inputs and two outputs. Label the data, clock, set and reset inputs, d, c, s, and r, respectively. Active s or r inputs override the clocked values on the d input; s and r cannot simultaneously be active. Changes on d when c is low have no effect on the q and qb outputs of the latch.

a. (3 points) Write an entity.

b. (7 points) Write a synthesizable behavioral architecture.

11. (20 points) Specify type declarations for the following data types.

a. (3 points) A four valued logic system, `MVL4`, with values '0', '1', 'X', and 'Z'. Values '0' and '1' have the usual logic meaning. Value 'Z' means high impedance state and 'X' means unknown. Any uninitialized data item of this type should have value 'X'.

b. (3 points) A `DAY_OF_WEEK` enumeration data type.

c. (2 points) A data type `BUFFER_NUMBER` that can have integer values in the range from 0 to 7.

d. (2 points) A data type `COST` that can have real values between $0.00 and $1,405.00.

e. (2 points) A descending range data type `DEC_16` with integer values from 15 to 0.

f. (4 points) A 16-bit descending-index register composite data type, `REG_16_DESCENDING`, with index valued from the type `DEC_16` declared above, and component values of type MVL4.

g. (4 points) A three-dimensional table, `TABLE_3D`, with index values and table entries all of type `std_logic` (which has been declared elsewhere and is visible).

12. (1 point) An entity X, when used in another entity, becomes a _____ for the entity Y.

13. (1 point) _____ is an example of an unconstrained array.

14. (10 points) Draw the state diagram for the following state machine. Is it a Moore machine or a Mealy machine?

```
ENTITY state_machine IS
   PORT (sig_in ; IN BIT; clk : IN BIT;
         sig_out : OUT BIT);
END state_machine;

ARCHITECTURE state_machine OF state_machine IS
   TYPE state_type IS (a, b, c, d, e);
   SIGNAL current_state, next_state : state_type;
BEGIN
   PROCESS (sig_in, current_state)
   BEGIN
      sig_out <= '0';
      next_state <= e;
      CASE current_state
      WHEN a =>
         IF sig_in = '0' THEN
            next_state <= a;
          sig_out <= '1';
         ELSE
            next_state <= d;
         END IF;
       WHEN b =>
         IF sig_in = '0' THEN
            next_state <= b;
         ELSE
            next_state <= c;
          sig_out <= '1';
         END IF;
     WHEN c =>
       IF sig_in = '1' THEN
           sig_out <= '1';
           next_state <= a;
       ELSE
          next_state <= e;
       END IF;
     WHEN d =>
       IF sig_in = '0' THEN
           sig_out <= '1';
           next_state <= e;
       END IF;
     WHEN e =>
       IF sig_in = '1' THEN
          next_state <= c;
       END IF;
      END CASE;
   END PROCESS;
   PROCESS (clk)
   BEGIN
      IF (clk'EVENT AND clk = '1') THEN
      current_state <= next_state;
      END IF;
   END PROCESS;
END state_machine;
```