CPE/EE 422/522

Introduction to Xilinx Virtex Field-Programmable Gate Arrays Devices

Dr. Rhonda Kay Gaede

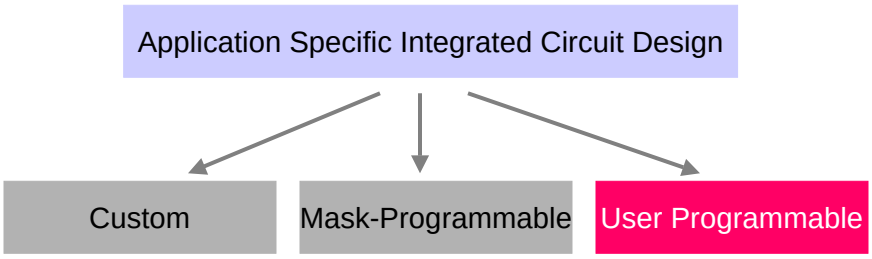
UAH

Electrical and Computer Engineering

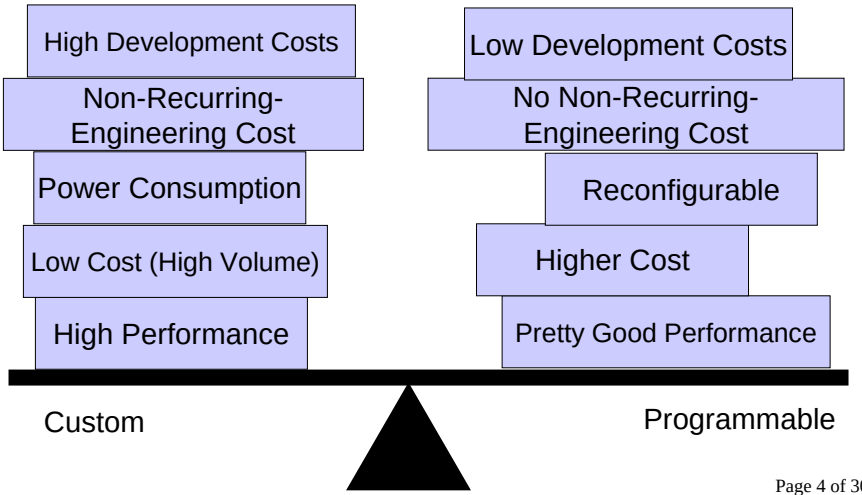
Outline

- Introduction
- Field-Programmable Gate Arrays
- Virtex
- Virtex-E, Virtex-II, and Virtex-II Pro

The World of Application Specific Integrated Circuit Design



Selecting a Technology

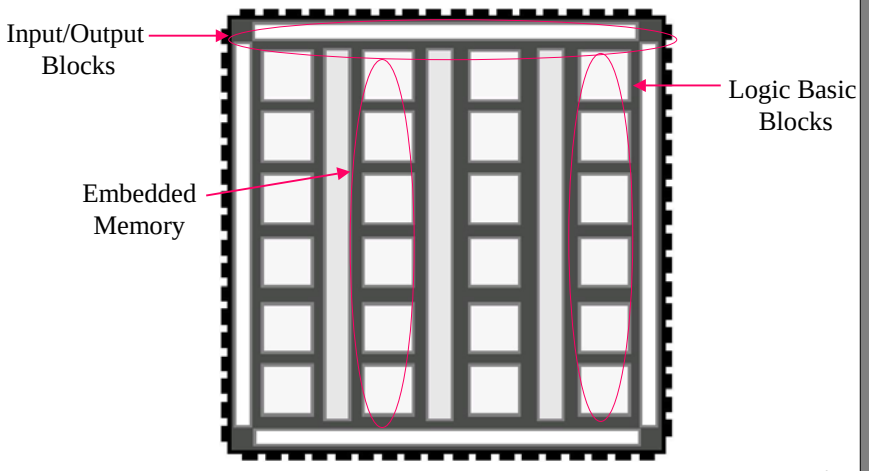


What is an FPGA?

What are FPGAs made of?

- FPGA: Field-Programmable Gate Arrays
  - Basic blocks of logic function (CLBs)
  - Programmable input/output blocks (IOBs)
  - Programmable interconnections
  - Embedded memory (bRAMs)
- Type of interconnections network
  - Anti-fuse
  - SRAM

Basic Layout of an FPGA



Xilinx Virtex 2.5V FPGA (1)

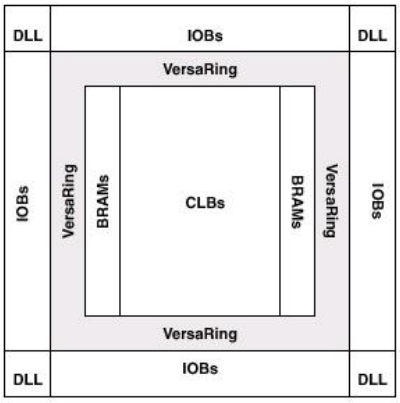
- Densities from 50k to 1M system gates
- System performance up to 200 MHz
- Four dedicated delay-locked loops (DLLs) for advanced clock control
- Dedicated carry logic for high-speed arithmetic
- Look-up-table based architecture
- IEEE 1149.1 boundary-scan logic
- SRAM-based in-system configurable
- Unlimited re-programmability
- 0.22 μm 5-layer metal process
- Number of user I/O pins range from 94 to 512

Xilinx Virtex 2.5V FPGA (2)

Virtex Field-Programmable Gate Array Family Members

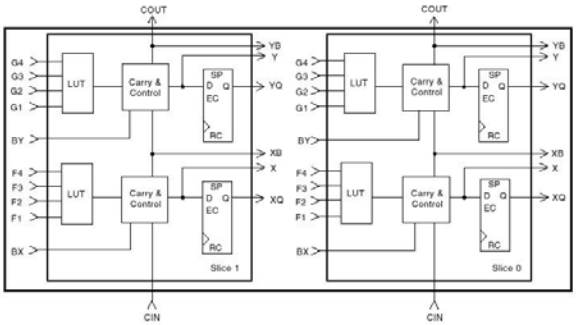
Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Maximum SelectRAM+™ Bits
XCV50	57,906	16x24	1,728	180	32,768	24,576
XCV100	108,904	20x30	2,700	180	40,960	38,400
XCV150	164,674	24x36	3,888	260	49,152	55,296
XCV200	236,666	28x42	5,292	284	57,344	75,264
XCV300	322,970	32x48	6,912	316	65,536	98,304
XCV400	468,252	40x60	10,800	404	81,920	153,600
XCV600	661,111	48x72	15,552	512	98,304	221,184
XCV800	888,439	56x84	21,168	512	114,688	301,056
XCV1000	1,124,022	64x96	27,648	512	131,072	393,216

Xilinx Virtex 2.5V FPGA (3)

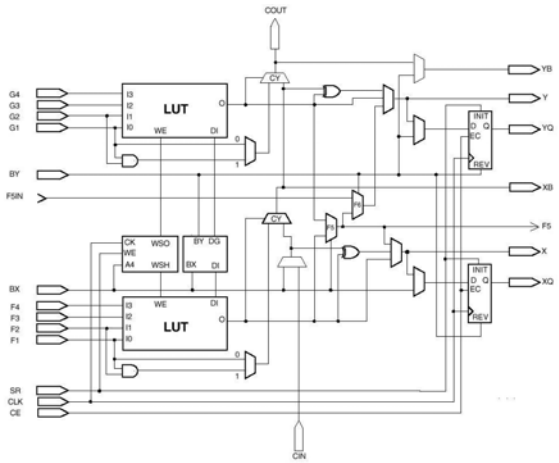


CLB: Configurable Logic Block (1)

- The Logic Cell (LC) is the basic building block of the Virtex CLB
- LC includes
  - 4-input function generator
  - carry logic
  - storage element
- CLB = 4 LCs

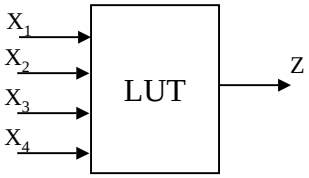


Virtex Slice



LUT: Look Up Table

- Basic building blocks of a logic function
- Virtex contains 4-input LUT
- Capacity limited by number of input
- Configures as LUT, ROM, and RAM

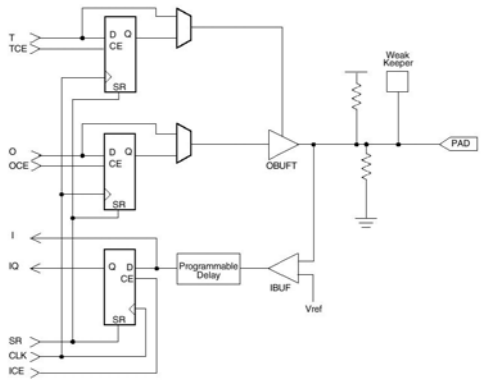


Example:
$Z = X_1X_2 + X_3 + X_4$

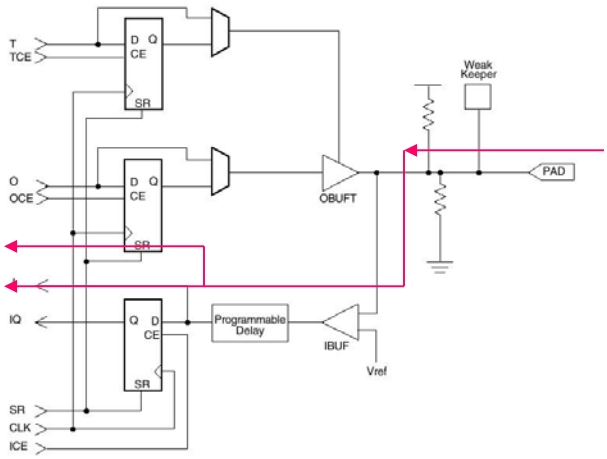
X_1	X_2	X_3	X_4	Z
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1
1	1	1	1	1

IOB: Input/Output Block

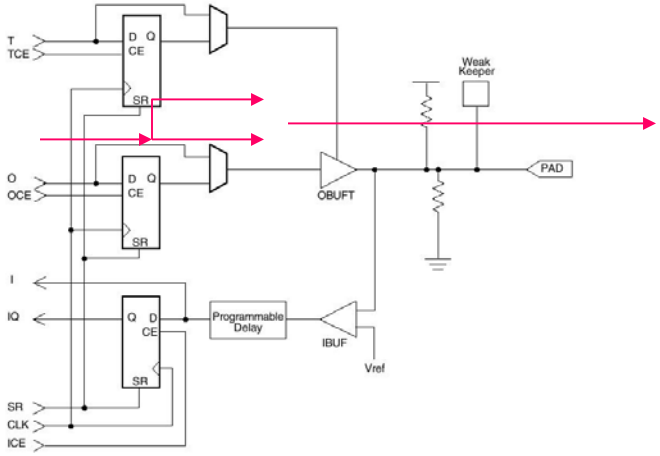
- Interface between pins and CLBs
- Supports wide variety of I/O signalling standards



Input



Output

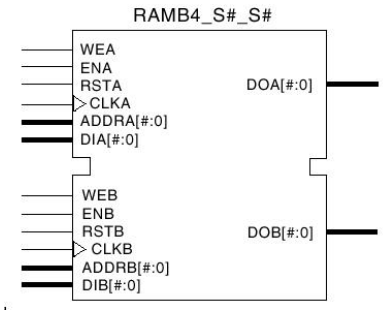


Compatible Output Standards

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

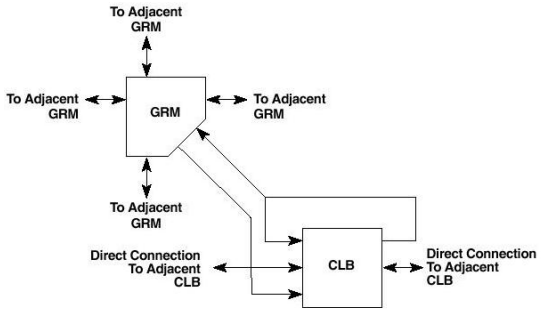
Embedded Memory

- Two Types
  - Block RAM
  - Block SelectRAM



Programmable Routing Matrix (1)

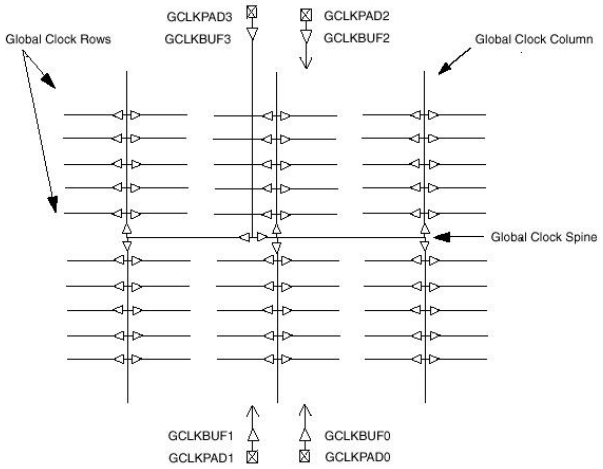
- Quality of routing controls the speed of a design
- Local Routing:
  - CLB feedback paths
  - Chains horizontal CLBs together



Programmable Routing Matrix (2)

- General Routing
  - General Routing Matrix (GRM)
  - Horizontal and vertical routing resources
  - 24 single-length lines in each of the four directions
  - 12 longlines (horizontal and vertical)
- VersaRing: interface between the CLBs and IOBs – pin-swapping and pin-locking
- Global Routing: 4 dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew
- Delay-Locked Loop: eliminate skew between the clock input pad and internal clock-input pins throughout the device

Programmable Routing Matrix (3)



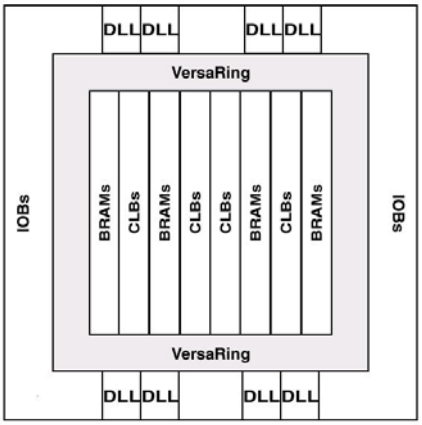
Direction of Technology

- ?

Device Release Dates

- Virtex, November 1998
- Virtex-E, December 1999
- Virtex-II, November 2000
- Virtex-II Pro, January 2002

Virtex-E

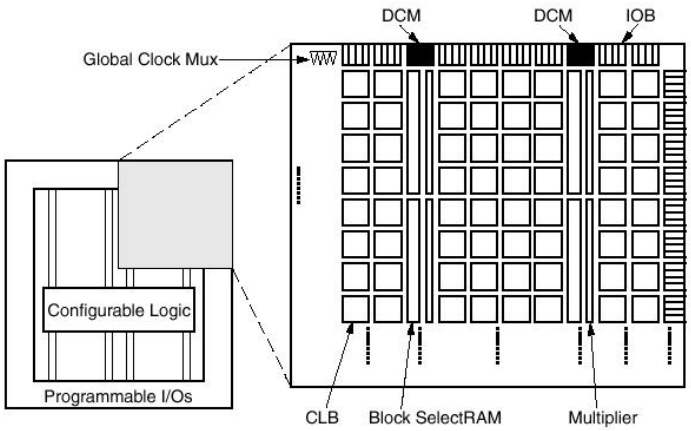


Virtex-E

Virtex-E Field-Programmable Gate Array Family Members

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	196	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

Virtex-II

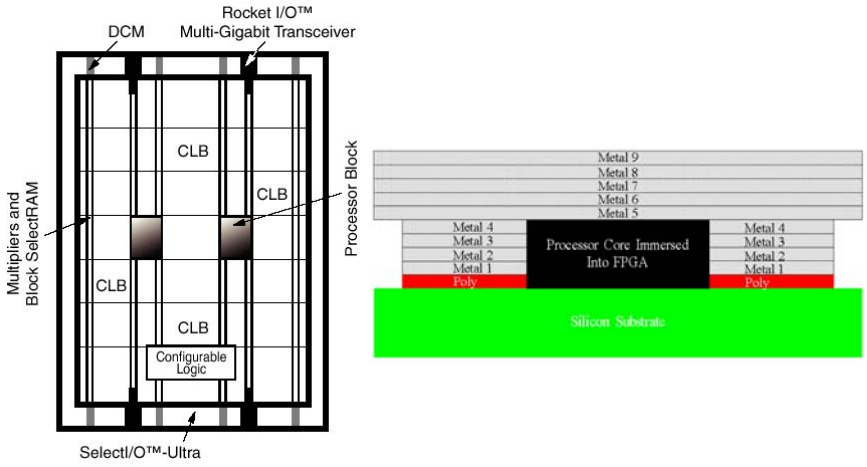


Virtex-II

Virtex-II Field-Programmable Gate Array Family Members

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits) Array Row x Col.	Slices	Maximum Distributed RAM Kbits	Multiplier Blocks	SelectRAM Blocks 18 Kbit Blocks	Max RAM (Kbits)	DCMs	Max I/O Pads(1)
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

Virtex-II Pro



Virtex-II Pro

Virtex-II Pro FPGA Family Members

Device	Rocket I/O Transceiver Blocks	PowerPC Processor Blocks	Logic Cells[1]	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0[2] or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0[2] or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VP100	0[2] or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164
XC2VP125	0[2], 20, or 24	4	125,136	55,616	1,738	556	556	10,008	12	1,200

Notes:
1. Logic Cell = (1) 4-input LUT + (1)FF + Carry Logic
2. These devices can be ordered in a configuration without Rocket I/O transceivers. See Table 3 for package configurations.

Problems and Challenges

How to best utilize this pre-fabricated reconfigurable black-box?