CPE/EE 422/522

Chapter 3 - Designing with Programmable Logic Devices

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UAH

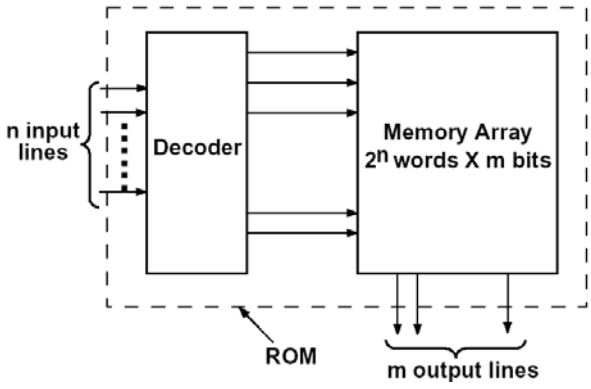
Programmable Logic Devices

- Read Only Memories (ROMs)
- Programmable Logic Arrays (PLAs)
- Programmable Array Logic Devices (PALs)

3.1 Read-Only Memories

- Store binary data
  - _____
  - _____
- n input lines, m output lines => array of 2n m-bit words
  - _____
- Use ROM to implement logic functions?
  - _____

3.1 Read-Only Memories - Basic ROM Structure

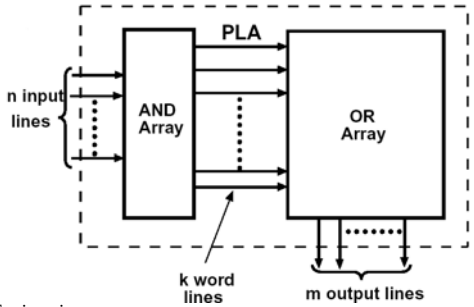


3.1 Read-Only Memories - ROM Types

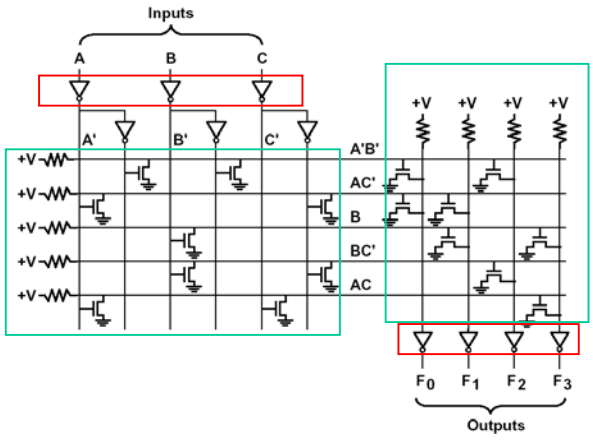
- Mask-programmable ROM
  - _____
  - _____
- EPROM (Erasable Programmable ROM)
  - _____
  - _____
  - _____
  - EEPROM – Electrically Erasable PROM
    - _____
  - Flash memories - similar to EEPROM except they use a different charge-storage mechanism
    - usually have built-in programming and erase capability, so the data can be written to the flash memory while it is in place, without the need for a separate programmer

3.2 Programmable Logic Arrays (PLAs)

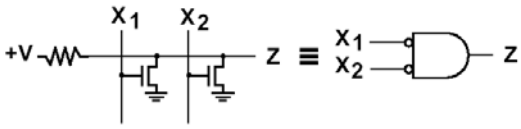
- Perform the same function as a ROM
  - *n* inputs and *m* outputs – _____
  - AND array – _____
  - OR array – _____



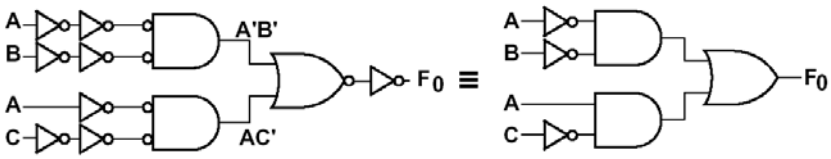
3.2 Programmable Logic Arrays - Example



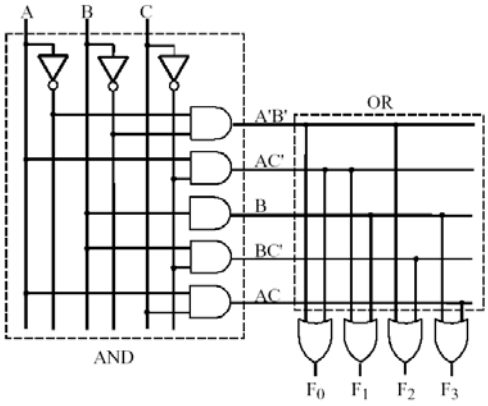
3.2 Programmable Logic Arrays - nMOS NOR Gate



$$F_0 = \sum m(0,1,4,6) = A'B' + AC'$$



3.2 Programmable Logic Arrays - AND-OR Array Equivalent



Modified Truth Table for PLA

$F_0 = \sum m(0,1,4,6) = A'B' + AC'$

$F_1 = \sum m(2,3,4,6,7) = B + AC'$

$F_2 = \sum m(0,1,2,6) = A'B' + BC'$

$F_3 = \sum m(2,3,5,6,7) = AC + B$

- 0 – variable is complemented
- 1 – variable is not complemented
- - – not present in the term

Product Term	Inputs			Outputs			
	A	B	C	F0	F1	F2	F3
A'B'	0	0	-	1	0	1	0
AC'	1	-	0	1	1	0	0
B	0	1	-	0	1	0	1
BC'	-	1	0	0	0	1	0
AC	1	-	1	0	0	0	1

Using PLA: An Example

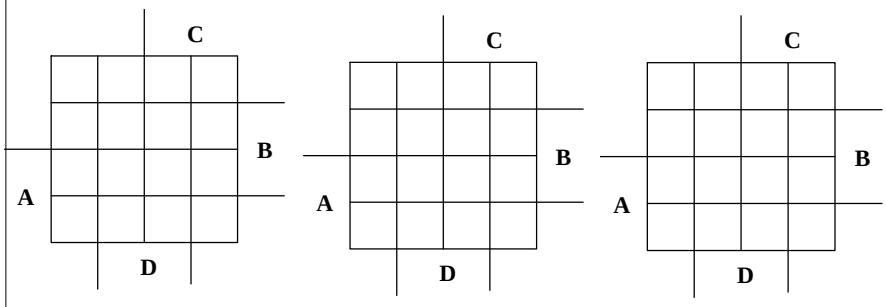
$F_1 = \sum m(2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$
$F_2 = \sum m(2, 3, 5, 6, 7, 10, 11, 14, 15)$
$F_3 = \sum m(6, 7, 8, 9, 13, 14, 15)$

$F_1 = bd + b'c + ab'$
$F_2 = c + a'bd$
$F_3 = bc + ab'c' + abd$

Eight different product terms are required!?

For PLA we want to minimize
the total number of product terms,
not the number of product terms for each function separately!

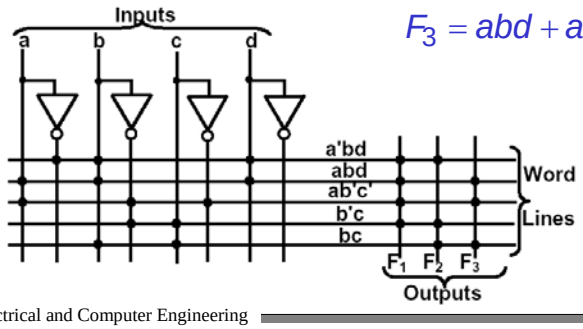
3.2 Programmable Logic Arrays - How Many Product Terms are Needed?



Using PLA: An Example

a	b	c	d	F_1	F_2	F_3
0	1	–	1	1	1	0
1	1	–	1	1	0	1
1	0	0	–	1	0	1
–	0	1	–	1	1	0
–	1	1	–	0	1	1

$$F_1 = a'bd + abd + ab'c' + b'c$$
$$F_2 = a'bd + b'c + bc$$
$$F_3 = abd + ab'c' + bc$$

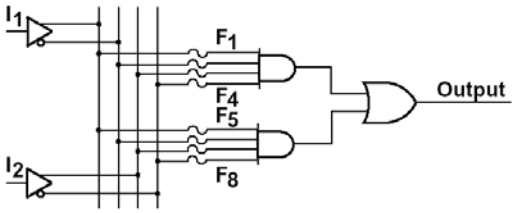


3.3 Programmable Array Logic (PALs)

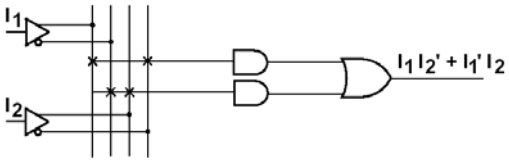
- PAL is a special case of PLA
  - AND array is _____ and OR array is _____
- PAL is
  - less expensive
  - easier to program

3.3 Programmable Array Logic (PALs)

Unprogrammed

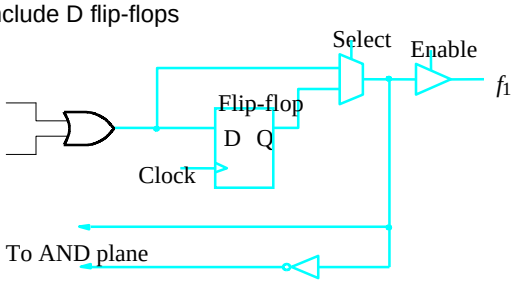


Programmed

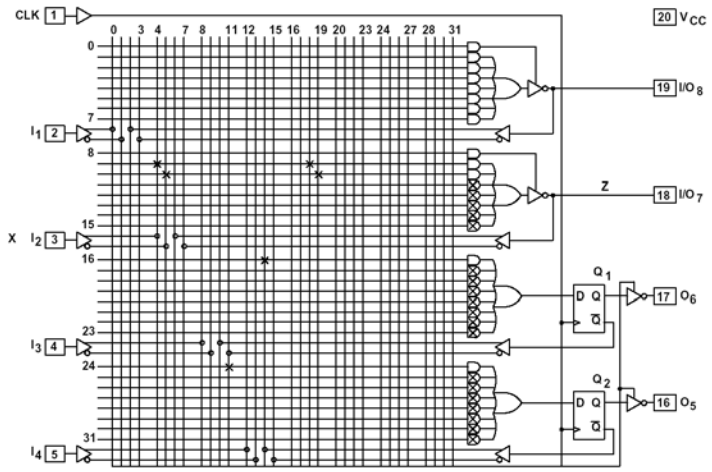


3.3 Programmable Array Logic - Specifications

- Typical PALs have
  - from 10 to 20 inputs
  - from 2 to 10 outputs
  - from 2 to 8 AND gates driving each OR gate
  - often include D flip-flops



3.3 Programmable Array Logic - Logic Diagram for 16R4 PAL - Top Half



3.3 Programmable Array Logic - Example