

**The University of Alabama in Huntsville
Electrical and Computer Engineering Department
CPE 221 01
Sample Final Exam
Spring 2018**

This test is closed book, closed notes. You may use a calculator. You should have the ARM reference packet. You must show your work to receive full credit.

1. (1 point) A _____ is used to control the access to a bus from the output of a register.
2. (1 point) _____ uses cross-coupled transistors to store one bit of memory.
3. (1 point) _____ requires refreshing.
4. (1 point) The principle of _____ locality states that items close to an item referenced are likely to be referenced in the near future.
5. (1 point) (True or False) _____ A two-way set associative cache has two sets.
6. (3 points) In an ARM computer, r2 contains a value of --3621 in decimal. What is the binary value of r1 after this instruction is executed?
MVN r1, r2

7. (3 points) In an ARM computer, r2 contains a value of 1698 in decimal. What is the binary value of r1 after this instruction is executed?
NEG r1, r2

8. (2 points) In an ARM computer, r2 contains a value of -3621 in decimal while r3 contains a value of 1698 in decimal. What is the binary value of r1 after this instruction is executed?

OR r1, r2, r3

9. (6 points) A RISC processor executes the following code. There are data dependencies. A source operand cannot be used until it has been written.

```
LDR    r2, [r4]
STR    r6, [r2]
```

Assuming a five-stage pipeline (fetch (IF), operand fetch (OF), execute (E), memory access (M), and register write (W)), how many extra cycles are required to ensure that the correct value of r2 is available for the STR instruction?

10. (15 points) (a) (9 points) What are the values of the following registers when the program executes "B loop" for the sixth time? Answer in decimal.

(r5: _____ r6: _____ r2: _____

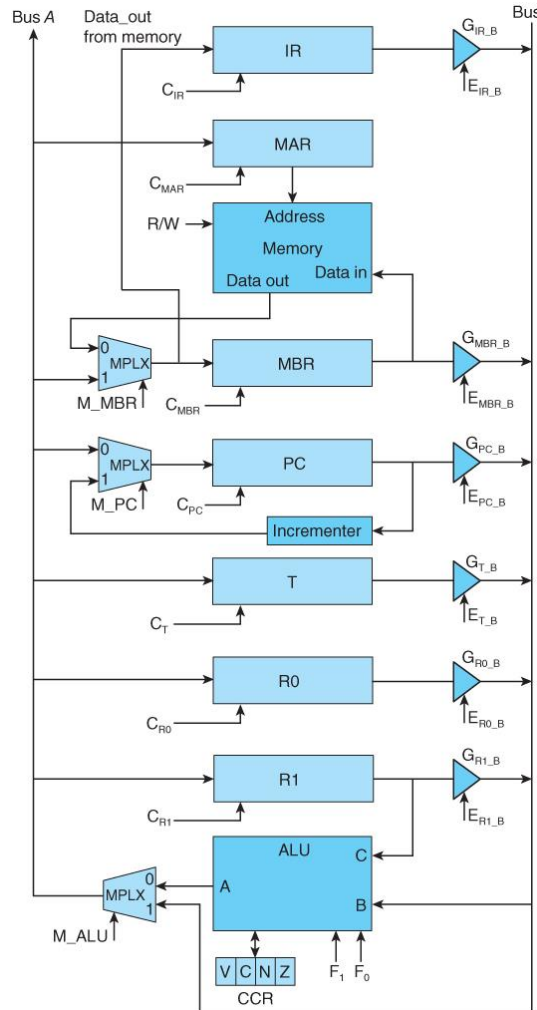
- (b) (6 points) Consider the STRGT and STRLE instructions that immediately precede the sixth execution of "B loop". What value is written by the STRGT instruction and what value is written by the STRLE instruction? Answer in decimal. STRGT _____ STRLE _____

```

AREA    PROB_11, CODE, READONLY
ENTRY
ADR     r0, x
ADR     r1, y
ADR     r2, z
LDR     r3, size
LDR     r4, i
loop    CMP     r4, r3
        BPL     done
        LDR     r5, [r0], #4
        LDR     r6, [r1], #4
        CMP     r5, r6
        STRGT  r5, [r2], #4
        STRLE  r6, [r2], #4
        ADD     r4, r4, #1
        B      loop
done    B      done
x       DCD    100, 3, -1, 2, 4, 4, 2, -1, 3, 100
y       DCD    -53, 247, 95, -7, 481, 91, -33, -1500, 29, -83
z       SPACE  40
i       DCD    0
size    DCD    10
END

```

11. (15 points) For the architecture shown, write the concrete RTL and the sequence of signals and control actions necessary to execute the instruction *STRI* (P), R0, R1, that stores the sum of D0 and D1 in the memory location pointed to by the contents of the memory location P. Assume that the address P is in the instruction register IR. Abstract RTL: $M[M[P]] \leftarrow R0 + R1$.



F ₁	F ₀	Operation
0	0	A = B + 1
0	1	A = B - 1
1	0	A = B + C
1	1	A = B - C

Cycle	Concrete RTL	Signals
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		

12. (10 points) A certain memory system has a 1024 MB main memory and a 64 MB cache. Blocks are 4 words and each word is 64 bits. Show the fields in a memory address if the cache is 16-way set associative.
13. (6 points) If you want to build a 2^{48} word, 64-bits-per-word memory and the only parts you have available to you are static RAM chips that contain 2^{40} 8 bit words each. (a) (2 points) How many rows are required? (b) (2 points) How many columns are required? (c) (2 points) How many chips in all?

15. (15 points) Consider the following ARM program. Trace the stack activity, including all changes to the stack pointer and to the contents of the stack. Clearly indicate the value of the sp.

```

0      MOV    sp, #0x00000000
4      B      main
8  swap  SUB    sp, sp, #4
12     LDR    r1, [sp, #8]
16     LDR    r2, [r1]
20     STR    r2, [sp]
24     LDR    r0, [sp, #4]
28     LDR    r3, [r0]
32     STR    r3, [r1]
36     LDR    r3, [sp]
40     STR    r3, [r0]
44     ADD    sp, sp, #4
48     MOV    pc, lr
52  main  SUB    sp, sp, #8
56     ADR    r6, x
60     STR    r6, [sp, #4]
64     ADR    r6, y
68     STR    r6, [sp]
72     BL    swap
76     ADD    sp, sp, #8
80  stop  B      stop
84  x     DCD    2
88  y     DCD    3
    
```

Address	Value
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction:

Address	Value
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction:

Address	Value
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction:

Address	Value
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction:

Address	Value
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction:

Address	Value
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction:

Address	Value
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction:

Address	Value
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction:

Address	Value
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction: