



**VLSI Design: Prelim Exam (01/21/2005)**

*Instructions: Answer all 5 questions. The exam includes 6 pages.*

**1. (20 points)**

**(a) (8 points)** Find the region of operation for each transistor assuming that  $V_{T0} = 0.4V$ . Fill in the following table.

	A	B	C	D
Operating mode				

**(b) (2 points)** (True | False) Transistor D has smaller  $V_T$  (threshold voltage) than transistor C. Circle the correct answer.

**(c) (4 points)** P-type transistors pass a logic  $\{0 | 1\}$  well, but pass a logic  $\{0 | 1\}$  poorly.

**(d) (4 points)** You would like to increase the noise margin for logic zero  $NM_L$  of a CMOS inverter. To achieve this you would increase the width of the (NMOS | PMOS) transistor. Circle the correct answer.

**(e) (2 points)** Write equation for switching power consumption for static CMOS logic.

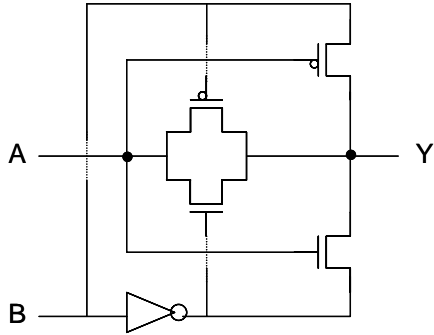
**2. (20 points)** Draw transistor level schematics for the following **static CMOS logic cells**. Clearly label the inputs (a, b, c, ...), the output (F), Vdd and Vss. Adjust the sizes of the transistors so that n-channel and p-channel stacks have equal strengths (the same drive strength as minimum-size inverter). Assume that the logic ratio is  $r = 3$ .

**(a) (10 points)** A 4-input NOR gate;

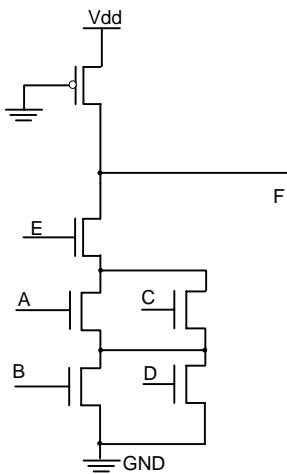
**(b) (10 points)** A gate that implements the function  $\overline{(ab + c)} \cdot d$ .

**3. (20 points)** For each of the circuits below, give the circuit style and the logic function implemented.

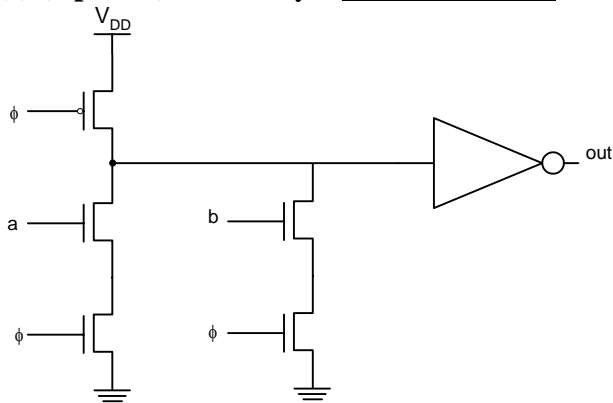
**(a) (5 points)** Circuit style: \_\_\_\_\_ Logic function:  $F =$  \_\_\_\_\_



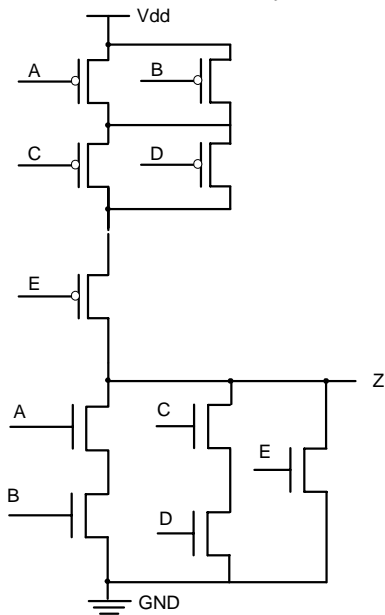
**(b) (5 points)** Circuit style: \_\_\_\_\_ Logic function:  $F =$  \_\_\_\_\_



**(c) (5 points)** Circuit style: \_\_\_\_\_ Logic function:  $F =$  \_\_\_\_\_



(d) (5 points) Circuit style: \_\_\_\_\_ Logic function:  $F =$  \_\_\_\_\_



4. (10 points)

(a) (5 points) For the following VHDL module give the full name of the network modeled with full description of control signals and draw an RTL (Register Transfer Level) schematic of the synthesized module.

```

library ieee;
use ieee.std_logic_1164.all;
entity mystery1 is
  port( D : in std_logic_vector(3 downto 0);
        Gn, Cl : in std_logic;
        Q : out std_logic_vector(3 downto 0));
end mystery1;

architecture arch1 of mystery1 is
begin
  process(Gn, Cl, D)
  begin
    if(Clr='1') then Q <= "0000";
    elsif(Gn='0') then Q <= D;
    end process;
end architecture arch1;

```

**(b) (5 points)** For the following VHDL module give the full name of the network modelled with full description of control signals and draw an RTL schematic of the synthesized module.

```
library ieee;
use ieee.std_logic_1164.all;

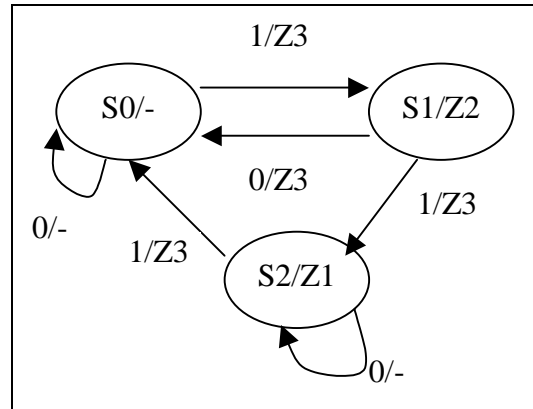
entity mystery2 is
  port(Clk, CLRb, SDR, SDL : in std_logic;
        S : in std_logic_vector(1 downto 0);
        D : in std_logic_vector(3 downto 0);
        Q : out std_logic_vector(3 downto 0));
end mystery2;

architecture arch1 of mystery2
  signal myS : std_logic_vector(3 downto 0);

begin
  process (Clk, CLRb)
  begin
    if (CLRb = '0')then
      Q <= "0000";
    elsif (Clk'event and Clk='0')then
      case S is
        when "11" => myS <= D;
        when "10" => myS <= SDR & Q(3 downto 1);
        when "01" => myS <= Q(2 downto 0) & SDL;
        when "00" => null;
      end case;
    end if;
  end process;
  Q <= myS;
end arch1;
```

**5. (30 points)** A simple sequential network is described using a state diagram shown on the right. The starting state is state S0.

Write a complete VHDL model for the network. What type of the sequential machine is this (Mealy or Moore)?



```

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
entity SM1 is
  port (
    CLK    : in  std_logic; -- clock signal
    X      : in  std_logic; -- input x
    Z      : out std_logic_vector(3 downto 1)); -- output vector Z3Z2Z1
end SM1;
architecture RTL of SM1 is
  --- write your code here

```



**VLSI Design: Prelim Exam (01/20/2006)**

*Instructions: Answer all 5 questions. The exam includes 5 pages.*

Q1 (20)	Q2 (20)	Q3 (20)	Q4 (20)	Q5 (20)	Total

**1. (20 points) Misc (Circuits)**

**(a) (4 points)** Find the region of operation for each transistor assuming that  $V_{T0} = 0.4V$ . Fill in the following table.

	A	B	C	D
Operating mode				

**(b) (2 points) (True | False)** Transistor D has smaller  $V_T$  (threshold voltage) than transistor C. Circle the correct answer.

**(c) (2 points) (True | False)** Current of transistor C is smaller than the current of transistor D. Circle the correct answer.

**(d) (2 points) (True | False)** Delay increases with the square of the number of transistors in the series. Circle the correct answer.

**(e) (2 points) (True | False)** Balancing delay paths in combination logic could help reduce power consumption. Circle the correct answer.

**(f) (4 points)** What are skewed gates? What are they good for?

**(g) (2 points) (True | False)** The ON current of a transistor increases with an increase in temperature. Circle the correct answer.

**(h) (2 points)** Write equation for the **switching power consumption** for static CMOS logic.

**2. (20 points)** Draw transistor level schematics for the following **static CMOS logic cells**. Clearly label the inputs (a, b, c, ...), the output (F), Vdd and Vss. Adjust the sizes of the transistors so that n-channel and p-channel stacks have equal strengths (the same drive strength as minimum-size inverter). Assume that the logic ratio is  $r = 3$ .

**(a) (10 points)** An AOI32 gate;

**(b) (10 points)** A gate that implements the function  $\overline{(a + b) \cdot cd}$ .

**3. (20 points)** Describe all techniques aimed at reducing power consumption (both leakage and active power). For each technique, explain is it design-time or run-time. Give pros and cons for each.

**4. (10 points) Sequential logic**

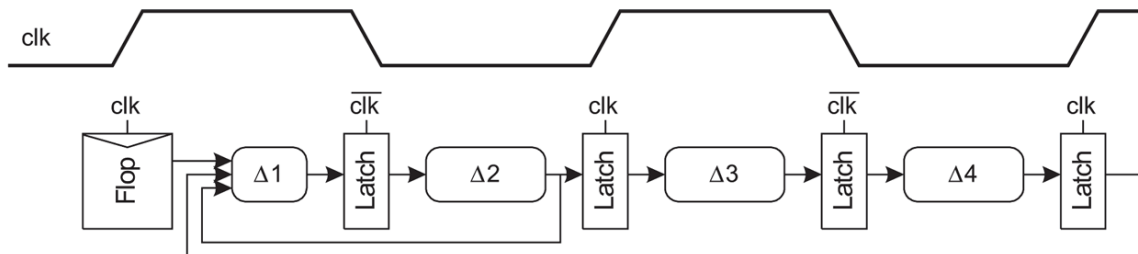
(a) (5 points) Give name and describe functionality of the following module described in Verilog HDL.

```
module XXX (C, CLR, Q);
input C, CLR;
output [3:0] Q;
reg [3:0] tmp;
always @(posedge C or posedge CLR)
begin
if (CLR)
tmp = 4'b0000;
else
tmp = tmp + 1'b1;
end
assign Q = tmp;
endmodule
```

(b) (15 points) Determine the minimum clock period at which the circuit in the figure below will operate correctly assuming logic delays from below. Assume the zero clock skew and that the latch delays are accounted for in the propagation delay  $\Delta$ 's.

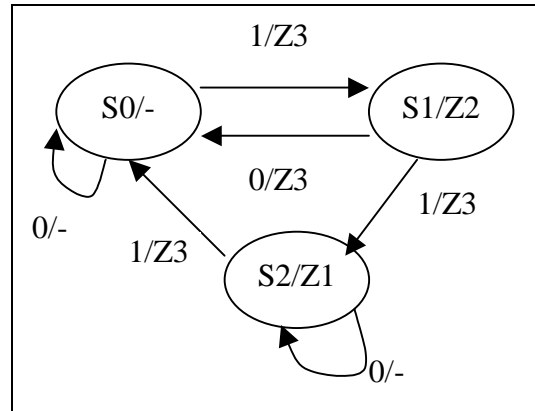
Note: In determining the minimum clock period, you can use time borrowing if applicable.

Logic delays:  $\Delta_1=300\text{ps}$ ,  $\Delta_2=400\text{ps}$ ,  $\Delta_3=200\text{ps}$ ,  $\Delta_4=350\text{ps}$ ?



**5. (20 points)** A simple sequential network is described using a state diagram shown on the right. The starting state is state S0.

Write a complete VHDL or Verilog model for the network. What type of the sequential machine is this (Mealy or Moore)?





**VLSI Design: Prelim Exam (01/18/2008)**

*Instructions: Answer all 5 questions. The exam has 7 pages.*

**1. (20 points)**

**(a) (8 points)** Find the region of operation for each transistor assuming that  $|V_{T0}| = 0.5V$ . Fill in the following table.

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
Operating mode				

**(b) (2 points) (True | False)** Transistor D has a smaller  $V_T$  (threshold voltage) than transistor B. Circle the correct answer.

**(c) (2 points) (True | False)** LO-skew gates will faster discharge the capacitive load than unskewed ones. Circle the correct answer.

**(d) (4 points)** A unit-sized inverter is driving unit sized inverters on a 32-bit datapath. Your task is to add inverters to buffer the signal. How many inverters you would add and what are their sizes?

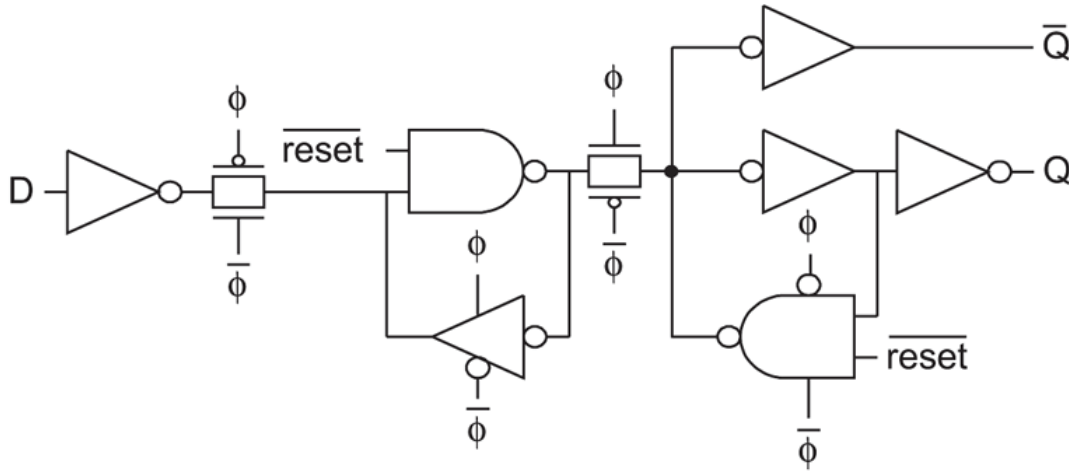
**(e) (4 points)** Write equation for probability of a 0 to 1 transition at the output of a 2-input NOR static CMOS gate as a function of input signal probabilities  $P_A$  and  $P_B$  ( $P_X$  is probability that signal X is equal to logic '1').

**2. (20 points)** Consider a 3-input NOR gate designed in static CMOS design style. Sketch transistor schematic and determine transistor sizes so that the worst-case pull-up and pull-down equivalent resistances are equal. Sketch the RC switch model and write equation for the gate delay for a “0 to 1” transition at the gate output.

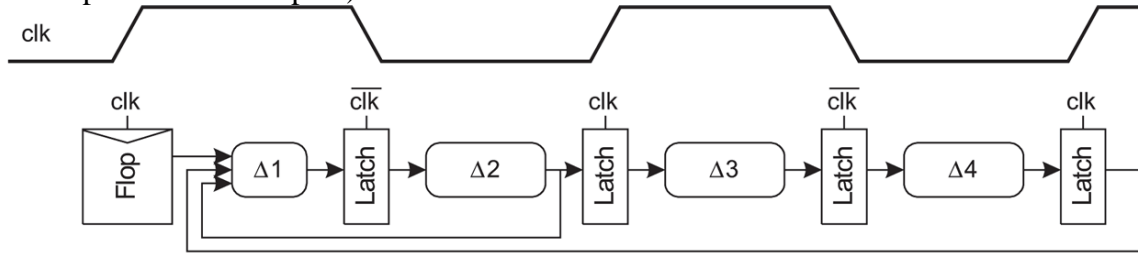


**4 (20 points). Sequential logic.**

**(a) (10 points).** Consider the following schematic. Give the function of this circuit and draw its corresponding schematic symbol. Calculate  $t_{\text{SETUP}}$ ,  $t_{\text{HOLD}}$ , and  $t_{\text{PCQ}}$ . Inverter delay is  $t_{\text{INV}}$ , clocked inverter delay is  $t_{\text{CINV}}$ , transmission gate delay is  $t_{\text{TG}}$ , NAND gate delay is  $t_{\text{NAND}}$ , and clocked NAND gate delay is  $t_{\text{CNAND}}$ .



**(b) (10 points) Sequencing.** Determine the minimum clock period at which the circuit in the figure below will operate correctly for each of the following logic delays. Assume the zero clock skew and that the latch delays are accounted for in the propagation delay  $\Delta$ 's.  
 Note: In determining the minimum clock period, you can use time borrowing if applicable (mind the return paths in the datapath).



**(b1) (5 points)**  $\Delta_1=400\text{ps}$ ,  $\Delta_2=440\text{ps}$ ,  $\Delta_3=500\text{ps}$ ,  $\Delta_4=500\text{ps}$ ?

**(b2) (5 points)**  $\Delta_1=600\text{ps}$ ,  $\Delta_2=900\text{ps}$ ,  $\Delta_3=400\text{ps}$ ,  $\Delta_4=550\text{ps}$ ?

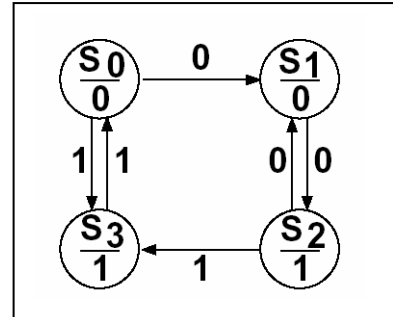
**5. (20 points)**

**(a) (10 points)** Write a generic VHDL model (the size is specified during instantiation) that describes a counter with the following characteristics. Signal Cln (Clear) is asynchronous and active low. All other state changes occur on the falling edge of the Clock signal. If the control inputs  $S0=S1=1$  the counter is loaded in parallel. If  $S0=0, S1 = 1$ , the counter counts up, if  $S0=1, S1=0$  it counts down. If  $S0=S1=0$ , no action occurs.

(b) (10 points) A simple sequential network is described using a state diagram shown on the right. The starting state is state S0.

Write a complete VHDL model for the network.

What type of the sequential machine is this (Mealy or Moore)?



```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
entity SM1 is
  port (
    CLK    : in  std_logic; -- clock signal
    a      : in  std_logic; -- input a
    y      : out std_logic; -- output x
  )
end SM1;
architecture RTL of SM1 is
  --- write your code here
```



**VLSI Design: Prelim Exam (01/16/2009)**

*Instructions: Answer all 5 questions. The exam has 7 pages.*

**1. (20 points)**

**(a) (8 points)** Find the region of operation for each transistor assuming that  $|V_{T0}| = 0.5V$ . Fill in the following table.

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
Operating mode				

**(b) (2 points) (True | False)** Transistor D has a smaller  $V_T$  (threshold voltage) than transistor B. Circle the correct answer.

**(c) (2 points) (True | False)** HI-skew gates will faster discharge the capacitive load than unskewed ones. Circle the correct answer.

**(d) (4 points)** A unit-sized inverter is driving unit sized inverters on a 16-bit datapath. Your task is to add inverters to buffer the signal. How many inverters you would add and what are their sizes?

**(e) (4 points)** Write equation for probability of a 0 to 1 transition at the output of a 2-input NAND static CMOS gate as a function of input signal probabilities  $P_A$  and  $P_B$  ( $P_X$  is probability that signal X is equal to logic '1').

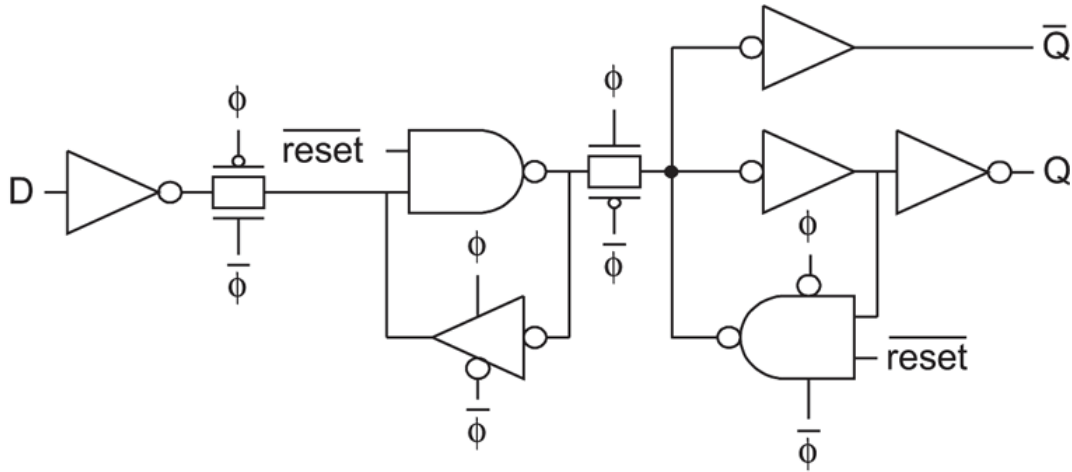
**2. (20 points)** Consider a 3-input AOI21 gate designed in static CMOS design style. Sketch transistor schematic and determine transistor sizes so that the worst-case pull-up and pull-down equivalent resistances are equal. Sketch the RC switch model and write equation for the gate delay for a “0 to 1” transition at the gate output.

**3. (20 points). Circuit styles.** Sketch the transistor schematics, annotate the sizes, and determine logical efforts ( $g_d$ ,  $g_u$ ,  $g_{avg}$ ) for the following logic gates and circuit styles.

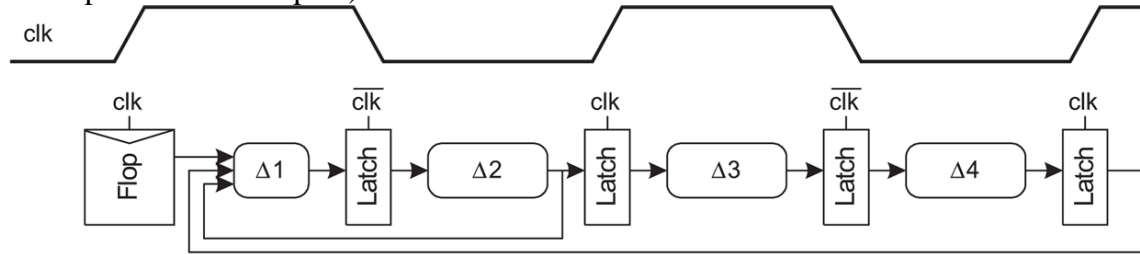
<p>(a) AOI21, pseudo-NMOS</p>	<p>(b) AND3, dynamic footed</p>
<p>(c) OAI32, static CMOS</p>	<p>(d) NAND2, HI-SKEW</p>

**4 (20 points). Sequential logic.**

**(a) (10 points).** Consider the following schematic. Give the function of this circuit and draw its corresponding schematic symbol. Calculate  $t_{\text{SETUP}}$ ,  $t_{\text{HOLD}}$ , and  $t_{\text{PCQ}}$ . Inverter delay is  $t_{\text{INV}}$ , clocked inverter delay is  $t_{\text{CINV}}$ , transmission gate delay is  $t_{\text{TG}}$ , NAND gate delay is  $t_{\text{NAND}}$ , and clocked NAND gate delay is  $t_{\text{CNAND}}$ .



**(b) (10 points) Sequencing.** Determine the minimum clock period at which the circuit in the figure below will operate correctly for each of the following logic delays. Assume the zero clock skew and that the latch delays are accounted for in the propagation delay  $\Delta$ 's.  
Note: In determining the minimum clock period, you can use time borrowing if applicable (mind the return paths in the datapath).



**(b1) (5 points)**  $\Delta_1=400\text{ps}$ ,  $\Delta_2=440\text{ps}$ ,  $\Delta_3=500\text{ps}$ ,  $\Delta_4=500\text{ps}$ ?

**(b2) (5 points)**  $\Delta_1=600\text{ps}$ ,  $\Delta_2=900\text{ps}$ ,  $\Delta_3=400\text{ps}$ ,  $\Delta_4=550\text{ps}$ ?

**5. (20 points)**

**(a) (10 points)** Write a VHDL model that describes a register file with the following characteristics. The register file has 32 (R0-R31) 32-bit registers. It has 2 read address ports RAP1 and RAP2 and one write address port WAP. A register specified by the address RAP1 is read to DO1 output lines, if a control signal RD1 is active. Similarly, a register specified by the address RAP2 is read to DO2 lines, if a control signal RD2 is active. A control signal WREN (write enable) is active if we want to write a value from DI lines to a register specified by the WAP address lines.

**(b) (10 points)** Design a simple state-machine that recognizes a serial bit pattern with **exactly 3** consecutive logic '1's on an input IN (e.g., the input bit stream '1110001111101110000' includes two such patterns, recognized in clock cycle 4 and 16). The state machine should generate a logic '1' for 1 clock cycle at an output line OUT, once the pattern is recognized.

Design the state machine (give transitions block diagram) and write a complete VHDL model for the state machine.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
entity SM1 is
  port (
    CLK      : in  std_logic; -- clock signal
    IN       : in  std_logic; -- input a
    OUT      : out std_logic;  -- output x
  )
end SM1;
architecture RTL of SM1 is
--- write your code here
```